

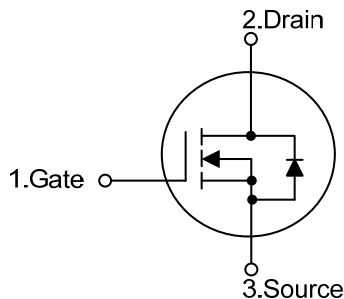
**UTT85N04****POWER MOSFET****85A, 40V N-CHANNEL
ENHANCEMENT MODE
TRENCH POWER MOSFET****DESCRIPTION**

The UTC **UTT85N04** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

The UTC **UTT85N04** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

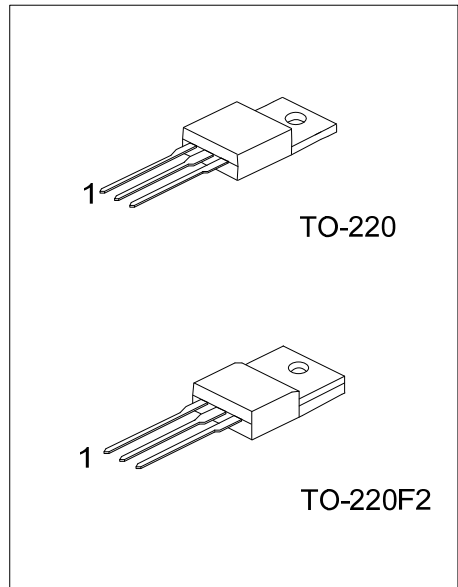
- * $R_{DS(ON)} \leq 3.7m\Omega$ @ $V_{GS}=10V$, $I_D=20A$
- * $R_{DS(ON)} \leq 4.3m\Omega$ @ $V_{GS}=4.5V$, $I_D=20A$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL**ORDERING INFORMATION**

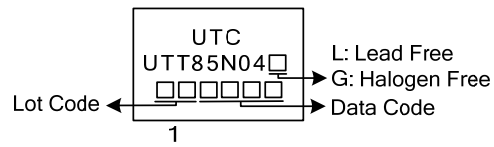
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT85N04L-TA3-T	UTT85N04G-TA3-T	TO-220	G	D	S	Tube
UTT85N04L-TF2-T	UTT85N04G-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: A: Anode K: Common Cathode NC: No Comment

UTT85N04G-TA3-T		(1)Packing Type	(1) T: Tube
		(2)Package Type	(2) TA3: TO-220, TF2: TO-220F2
		(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	85	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	400	A
Avalanche Current (Note 3)		I_{AR}	63	A
Avalanche energy	Single Pulsed (Note 3)	E_{AS}	200	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2	V/nS
Power Dissipation	TO-220	P_D	100	W
	TO-220F2		36	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=63\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$.

■ THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	1.25	$^{\circ}\text{C}/\text{W}$
	TO-220F2		3.47	$^{\circ}\text{C}/\text{W}$

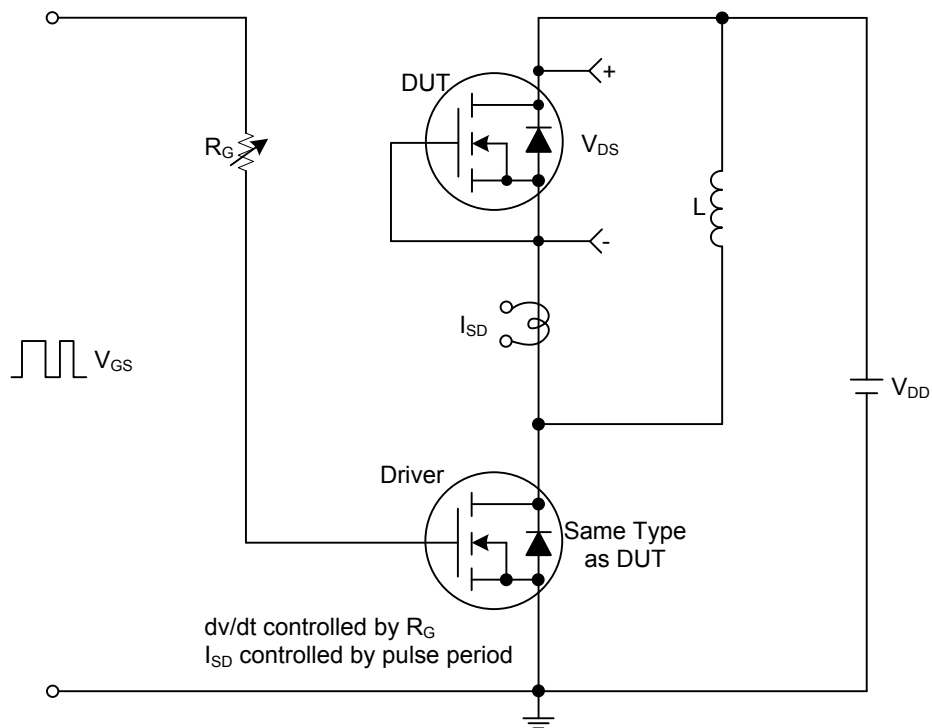
■ ELECTRICAL CHARACTERISTICS (T_A =25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A			3.7	mΩ
			V _{GS} =4.5V, I _D =20A			4.3	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =20V, f=1.0MHz		6450		pF
Output Capacitance		C _{OSS}			650		pF
Reverse Transfer Capacitance		C _{RSS}			455		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =50V, V _{GS} =10V, I _D =1.3A, I _D =100μA (Note 1, 2)		455		nC
Gate to Source Charge		Q _{GS}			25		nC
Gate to Drain Charge		Q _{GD}			50		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =30V, V _{GS} =10V, I _D =0.5A, R _G =25Ω (Note 1, 2)		150		ns
Rise Time		t _R			250		ns
Turn-off Delay Time		t _{D(OFF)}			1700		ns
Fall-Time		t _F			700		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				85	A
Maximum Body-Diode Pulsed Current		I _{SM}				340	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =1.0A, V _{GS} =0V			1.2	V
Reverse Recovery Time (Note 1)		t _{rr}	I _S =30A, V _{GS} =0V,		45		nS
Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μS		50		nC

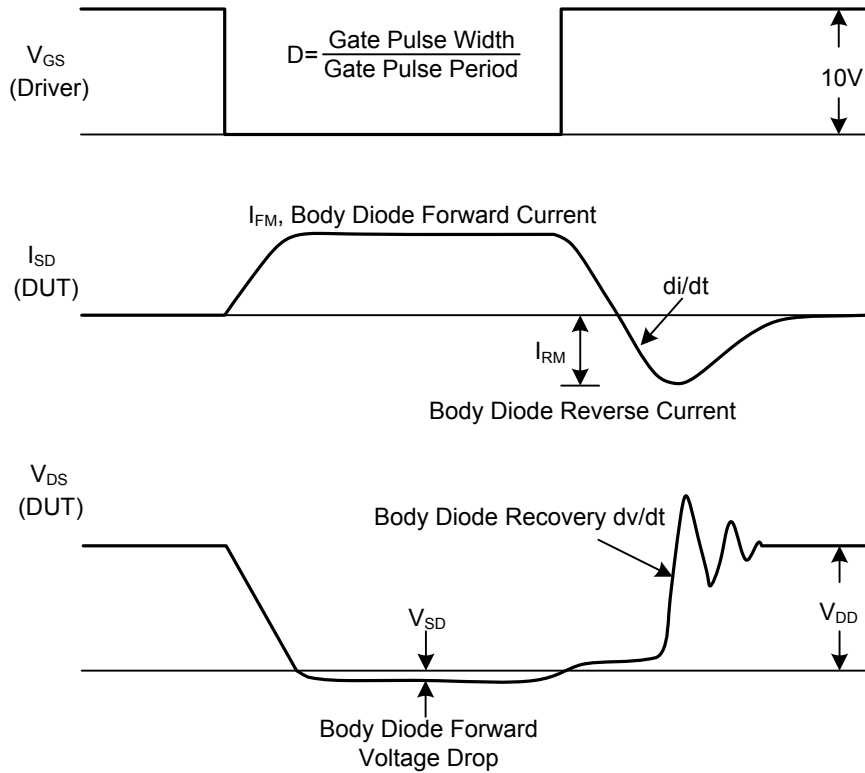
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



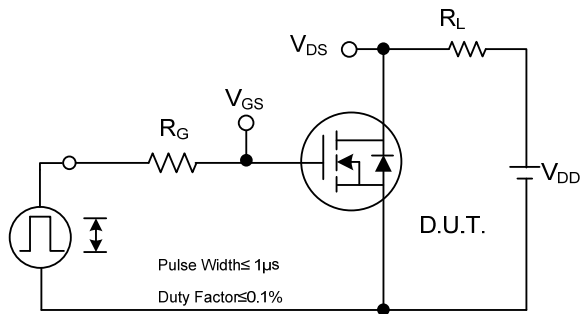
Peak Diode Recovery dv/dt Test Circuit



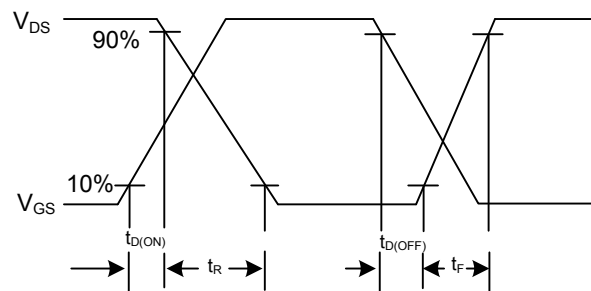
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

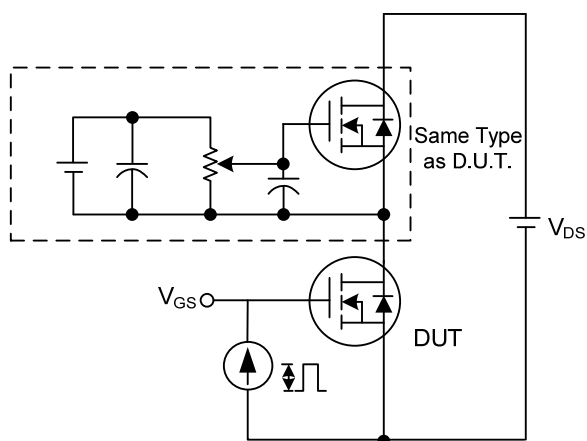
■ TEST CIRCUITS AND WAVEFORMS



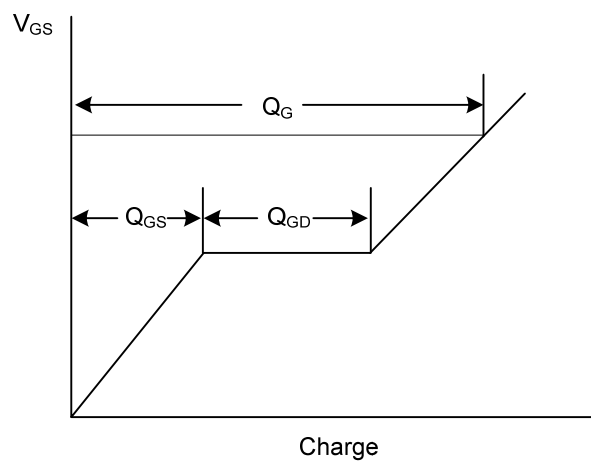
Switching Test Circuit



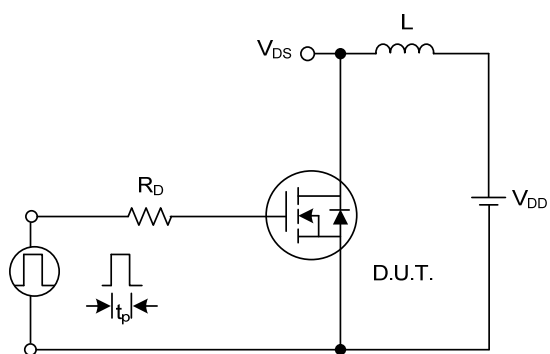
Switching Waveforms



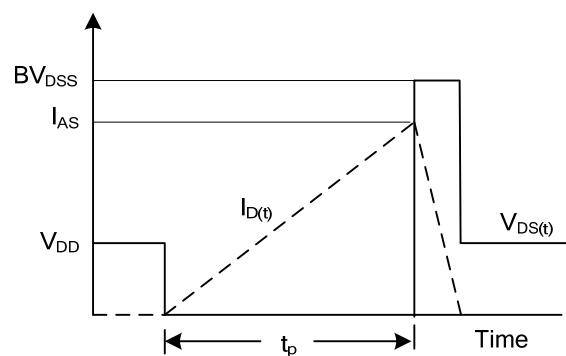
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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