



UTT12NP03

Power MOSFET

30V DUAL MIDDLE POWER MOSFET (N-CHANNEL/P-CHANNEL)

■ DESCRIPTION

The UTC **UTT12NP03** incorporates an N-channel MOSFET and a P-channel MOSFET, it uses UTC's advanced technology to provide customers a minimum on-state resistance and high-speed switching, thereby enabling high-density mounting.

The UTC **UTT12NP03** is universally applied in high-speed switching, motor driver.

■ FEATURES

* N-Channel

$$R_{DS(on)} \leq 26 \text{ m}\Omega @ V_{GS} = 10\text{V}, I_D = 5.8\text{A}$$

$$R_{DS(on)} \leq 31 \text{ m}\Omega @ V_{GS} = 4.5\text{V}, I_D = 5.0\text{A}$$

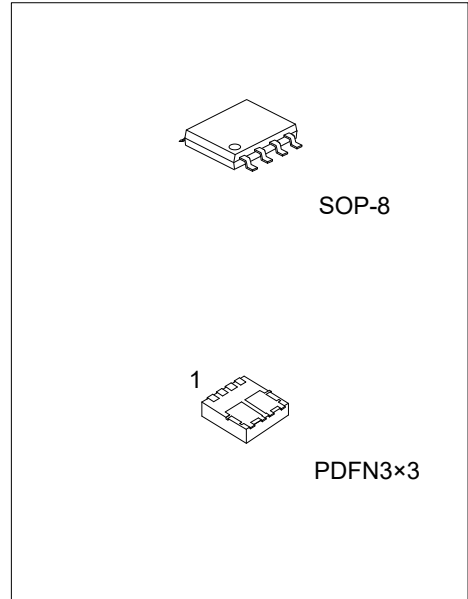
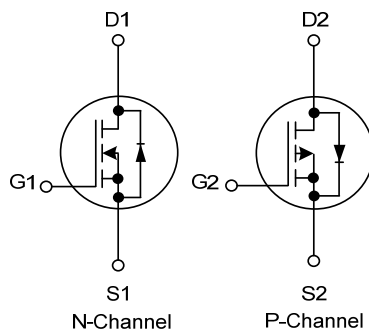
* P-Channel

$$R_{DS(on)} \leq 44 \text{ m}\Omega @ V_{GS} = -10\text{V}, I_D = -5.0\text{A}$$

$$R_{DS(on)} \leq 55 \text{ m}\Omega @ V_{GS} = -4.5\text{V}, I_D = -2.0\text{A}$$

* High switching speed

■ SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT12NP03L-S08-R	UTT12NP03G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel
UTT12NP03L-P3030-R	UTT12NP03G-P3030-R	PDFN3×3	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT12NP03G-S08-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) S08: SOP-8, P3030: PDFN3×3
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

SOP-8	PDFN3×3
8 7 6 5 UTC UTT12NP03 • 1 2 3 4 → Date Code → L: Lead Free → G: Halogen Free → Lot Code	UTT 12NP03 • → Date Code

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS		UNIT
			N-CH	P-CH	
Drain-Source Voltage		V _{DSS}	30	-30	V
Gate-Source Voltage		V _{GSS}	±10	±10	V
Drain Current	Continuous	I _D	8	-8	A
	Pulsed	I _{DM}	24	-24	A
Avalanche Energy, Single Pulse (Note 3)		E _{AS}	3	21	mJ
Power Dissipation	SOP-8	P _D	1.08		W
	PDFN3×3		15		W
Junction Temperature		T _J	+150		°C
Range of Storage Temperature		T _{STG}	-55 ~ +150		°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. N-Channel: L = 0.1mH, I_{AS} = 7.7A, V_{DD} = 25V, R_G = 25Ω, Starting T_J = 25°C

P-Channel: L = 0.1mH, I_{AS} = -20.5A, V_{DD} = -25V, R_G = 25Ω, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ _{JA}	125	°C/W
	PDFN3×3		75	°C/W
Junction to Case	SOP-8	θ _{JC}	115	°C/W
	PDFN3×3		8.3	°C/W

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^\circ\text{C}$, unless otherwise specified)

N-CHANNEL

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 10\text{V}$, $V_{DS}=0\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.5		2.0	V
Static Drain-Source On-State Resistance (Pulsed)	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=5.8\text{A}$			26	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=5.0\text{A}$			31	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1.0\text{MHz}$		489		pF
Output Capacitance	C_{OSS}			69		pF
Reverse Transfer Capacitance	C_{RSS}			59		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 2)	Q_G	$V_{GS}=10\text{V}$, $V_{DD}=24\text{V}$, $I_D=12\text{A}$ (Note 1, 2)		23		nC
Gate to Source Charge	Q_{GS}			5		nC
Gate to Drain Charge	Q_{GD}			5		nC
Turn-ON Delay Time (Note 2)	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		19		ns
Rise Time	t_R			24		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			290		ns
Fall-Time	t_F			121		ns
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Diode Forward Voltage	V_{SD}	$I_S=1.0\text{A}$, $V_{GS}=0\text{V}$			1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_S=12\text{A}$, $V_{GS}=0\text{V}$, $dI_F/dt=100\text{A}/\mu\text{s}$		73		nS
Body Diode Reverse Recovery Charge	Q_{rr}			35		nC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ ELECTRICAL CHARACTERISTICS (Cont.)

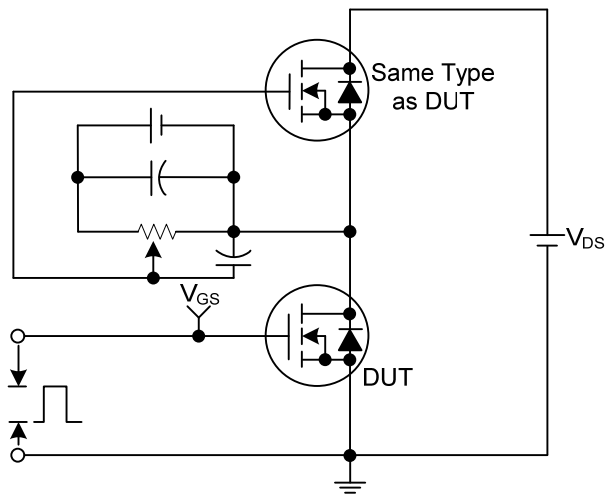
P-CHANNEL

Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

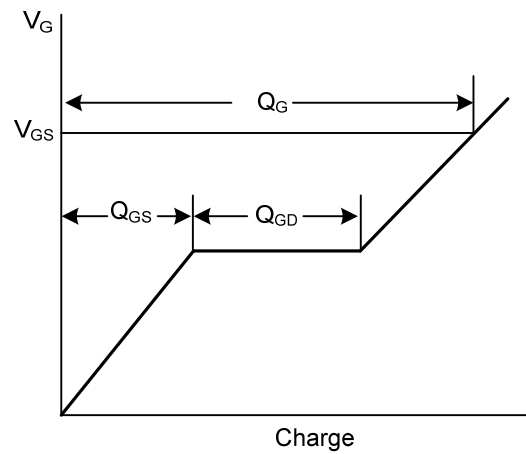
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

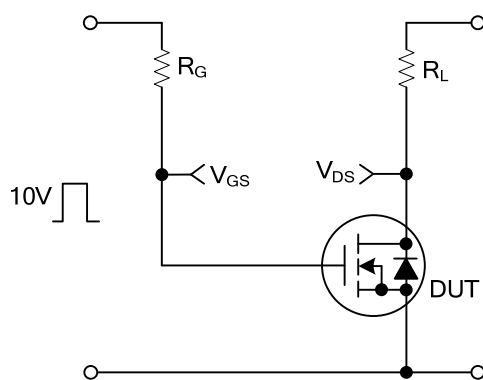
N-CHANNEL



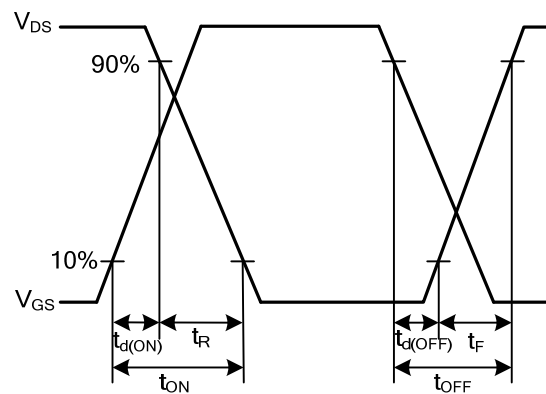
Gate Charge Test Circuit



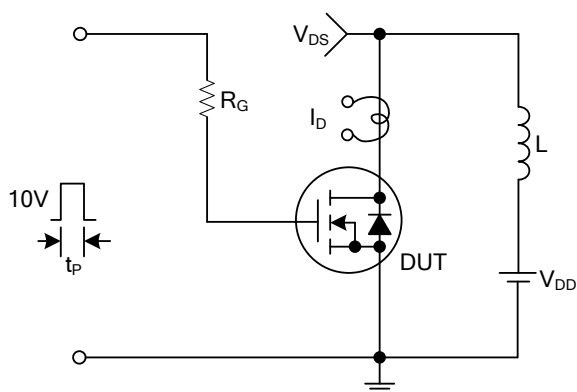
Gate Charge Waveforms



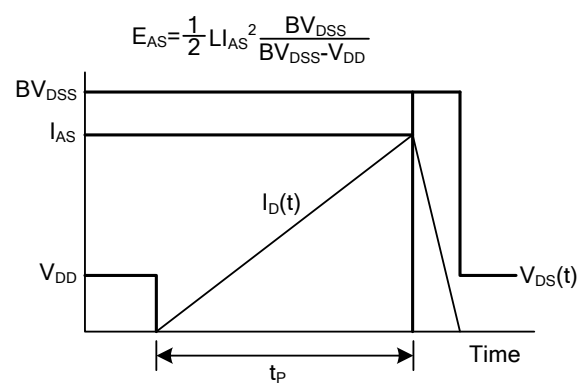
Resistive Switching Test Circuit



Resistive Switching Waveforms



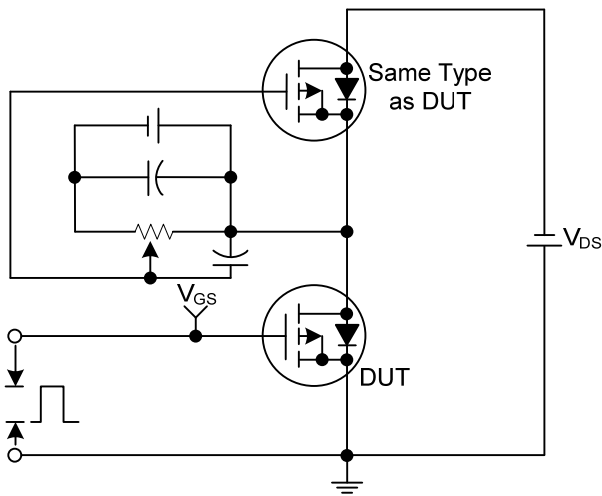
Unclamped Inductive Switching Test Circuit



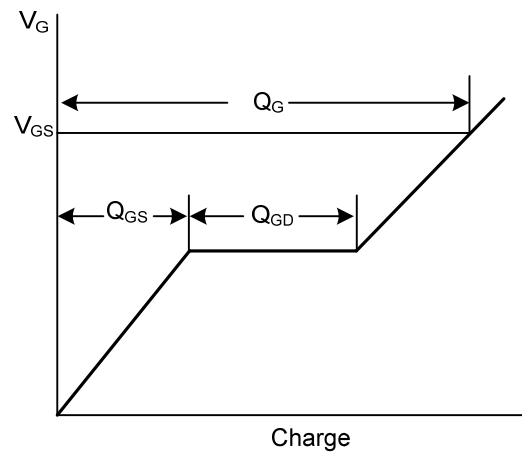
Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

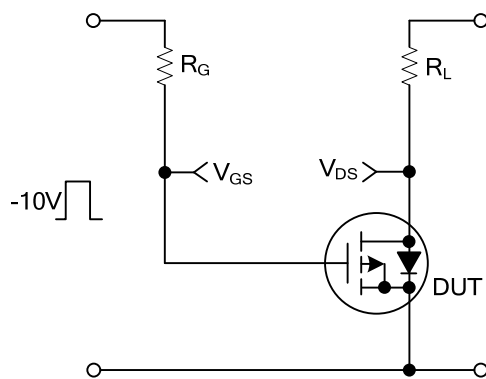
P-CHANNEL



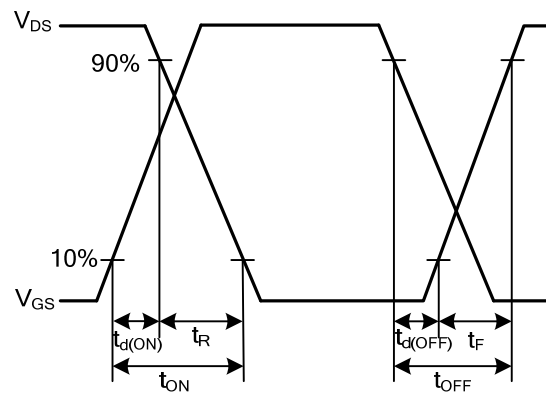
Gate Charge Test Circuit



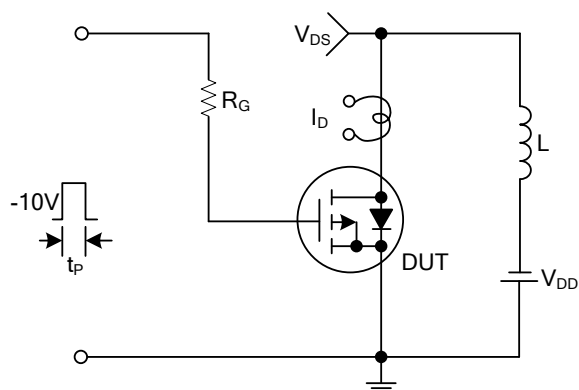
Gate Charge Waveforms



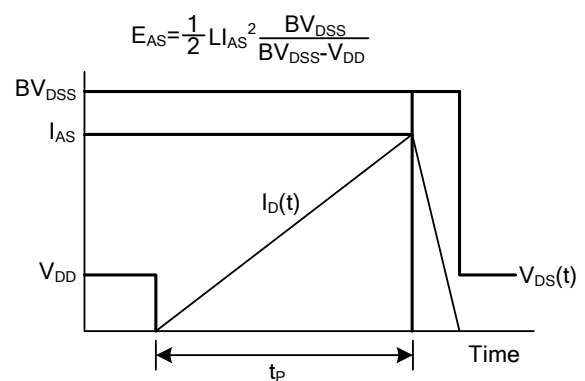
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.