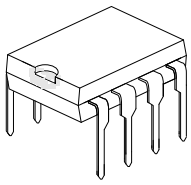
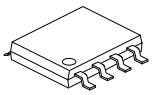
HALF-BRIDGE DRIVER



DIP-8



SOP-8

■ DESCRIPTION

The **UTR2103** is a high voltage, high speed power MOSF ET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600V.

■ FEATURES

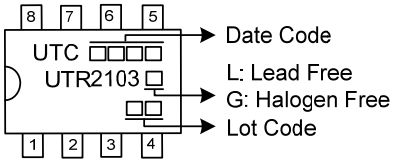
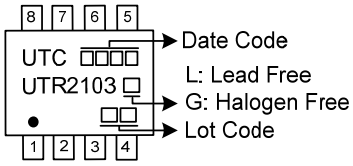
* Floating channel designed for bootstrap operation
* Fully operational to 600V
* Tolerant to negative transient voltage, dV/dt immune
* Gate drive supply range from 10V to 20V
* Undervoltage lockout
* 3.3V, 5V, and 15V input logic compatible
* Cross-conduction prevention logic
* Internally set deadtime
* High-side output in phase with HIN input
* Low-side output out of phase with $\overline{\text{LIN}}$ input
* Shutdown input turns off both channels
* Matched propagation delay for both channels

■ ORDERING INFORMATION

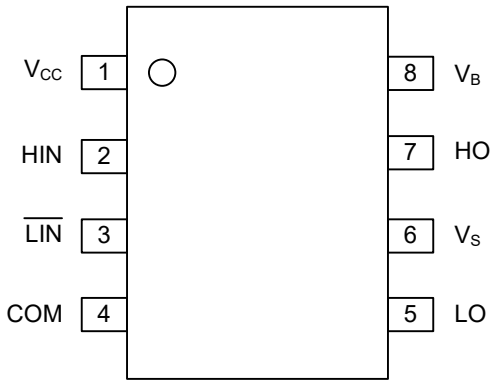
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UTR2103L-D08-T	UTR2103G-D08-T	DIP-8	Tube
UTR2103L-S08-R	UTR2103G-S08-R	SOP-8	Tape Reel

UTR2103G-D08-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

DIP-8	SOP-8
	

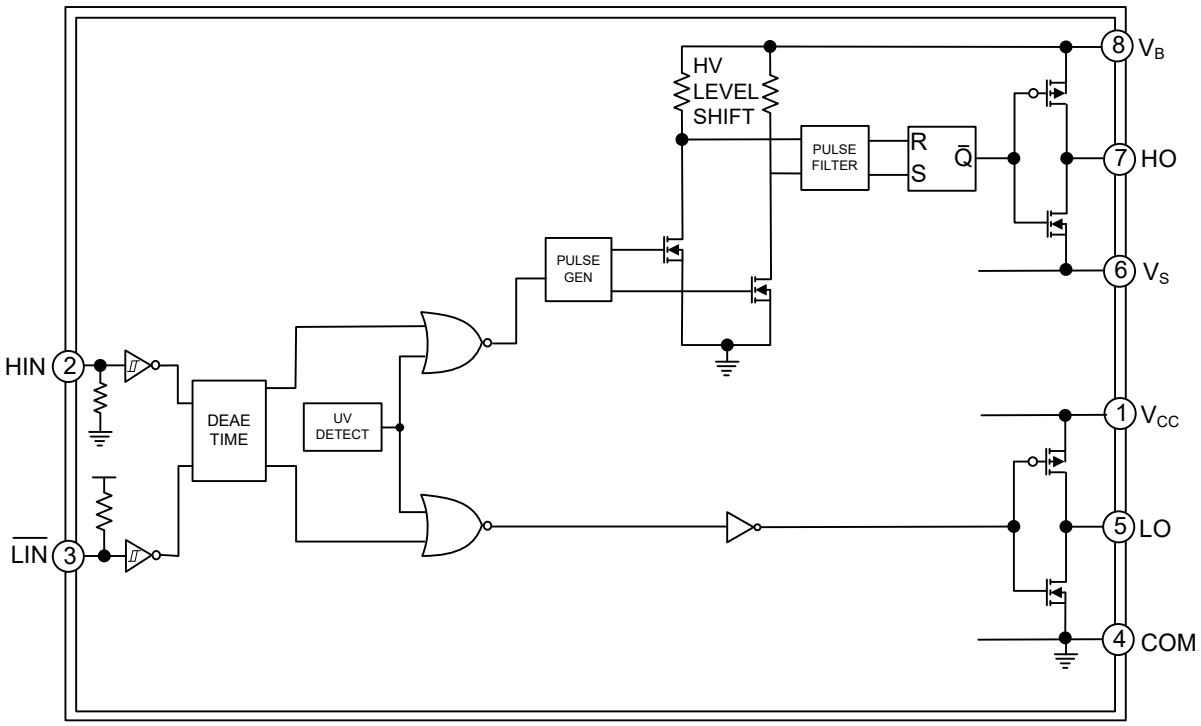
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{CC}	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	$\overline{LIN}$	Logic input for low-side gate driver output (LO), out of phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
High-Side Floating Absolute Voltage		V_B	-0.3 ~ 625	V
High-Side Floating Supply Offset Voltage		V_S	V_B-25 ~ V_B+0.3	V
High-Side Floating Output Voltage		V_{HO}	V_S-0.3 ~ V_B+0.3	V
Low-Side and logic Fixed Supply Voltage		V_{CC}	-0.3 ~ 25	V
Low-Side Output Voltage		V_{LO}	-0.3 ~ V_{CC}+0.3	V
Logic Input Voltage (HIN & $\overline{LIN}$)		V_{IN}	-0.3 ~ V_{CC}+0.3	V
Allowable Offset Supply Voltage Transient		dVs/dt	50	V/nS
Power Dissipation	DIP-8	P_D	1.0	W
	SOP-8		0.625	W
Maximum Junction Temperature		T_J	+150	°C
Maximum Storage Temperature Range		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

■ RECOMMENDED OPERATING RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
High-Side Floating Absolute Voltage	V_B	V_S+10 ~ V_S+20	V
High-Side Floating Supply Offset Voltage	V_S	600 (Note)	V
High-Side Floating Output Voltage	V_{HO}	V_S ~ V_B	V
Low-Side and logic Fixed Supply Voltage	V_{CC}	10 ~ 20	V
Low-Side Output Voltage	V_{LO}	0 ~ V_{CC}	V
Logic Input Voltage (HIN & $\overline{LIN}$)	V_{IN}	0 ~ V_{CC}	V
Ambient Temperature	T_A	-40 ~ +125	°C

Note: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to -V_{BS}.

■ THERMAL DATA

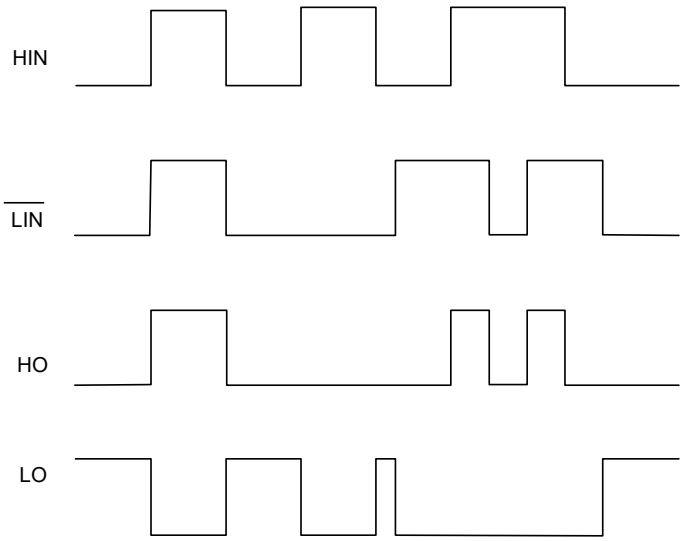
PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-8	θ_{JA}	125	°C/W
	SOP-8		200	°C/W

■ ELECTRICAL CHARACTERISTICS

[V_{BIAS} (V_{CC}, V_{BS})=15V and T_A=25°C unless otherwise specified. The V_{IN}, V_{TH}, and IIN parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Turn-ON Propagation Delay	t_{ON}	V_S=0V		880	980	ns
Turn-OFF Propagation Delay	t_{OFF}	V_S=600V		150	220	ns
Turn-ON Rise Time	t_r			70	170	ns
Turn-OFF Fall Time	t_f			35	90	ns
Delay matching, HS & LS Turn-ON/OFF	MT				60	ns
Deadtime, LS Turn-OFF to HS Turn-ON & HS Turn-ON to LS Turn-OFF	DT			720	850	ns
Logic “1” (HIN) & Logic “0” ($\overline{\text{LIN}}$) Input Voltage	V_{IH}	V_{CC}=10V~20V	2.5			V
Logic “0” (HIN) & Logic “1” ($\overline{\text{LIN}}$) Input Voltage	V_{IL}				0.8	V
High level Output Voltage, V_{BIAS} - V_O	V_{OH}	I_O=2mA		0.05	0.2	V
Low Level Output Voltage, V_O	V_{OL}			0.02	0.1	V
Offset Supply Leakage Current	I_{LK}	V_B=V_S=600V			50	μA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{IN}=0V or 5V		30	55	μA
Quiescent V_{CC} Supply Current	I_{QCC}			150	270	μA
Logic “1” Input Bias Current	I_{IN+}	V_{IN}=5V		3	10	μA
Logic “0” Input Bias Current	I_{IN-}	V_{IN}=0V			5	μA
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}		8	8.9	9.8	V
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}		7.4	8.2	9	V
Output High Short Circuit Pulsed Current	I_{O+}	V_{IN}=0V, V_O=0V	130	290		mA
Output Low Short Circuit Pulsed Current	I_{O-}	P_W≤10μs, V_O=15V	270	600		mA

■ TIMING DIAGRAM



■ TYPICAL APPLICATION CIRCUIT