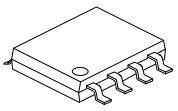
HIGH AND LOW SIDE DRIVER



SOP-8

■ DESCRIPTION

The **UTR2011** is a high power, high speed power MOSFET driver with independent high and low side referenced output channels. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 volts. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

■ FEATURES

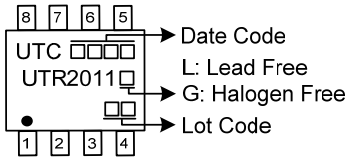
*Floating channel designed for bootstrap operation
*Fully operational to 200V
*Tolerant to negative transient voltage, dV/dt immune
*Gate drive supply range from 10V to 20V
*Independent low and high side channels
*Input logic HIN/LIN active high
*Undervoltage lockout for both channels
*3.3V and 5V logic compatible
*CMOS Schmitt-triggered inputs with pull-down
*Matched propagation delay for both channels

■ ORDERING INFORMATION

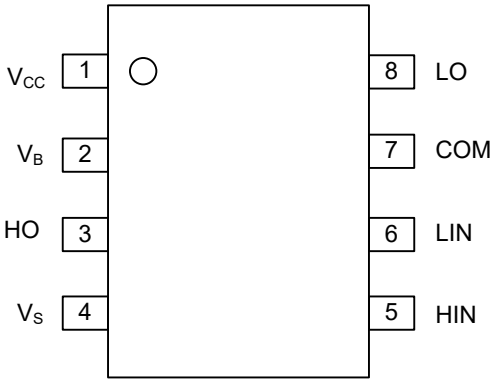
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UTR2011L-S08-R	UTR2011G-S08-R	SOP-8	Tape Reel

UTR2011G-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



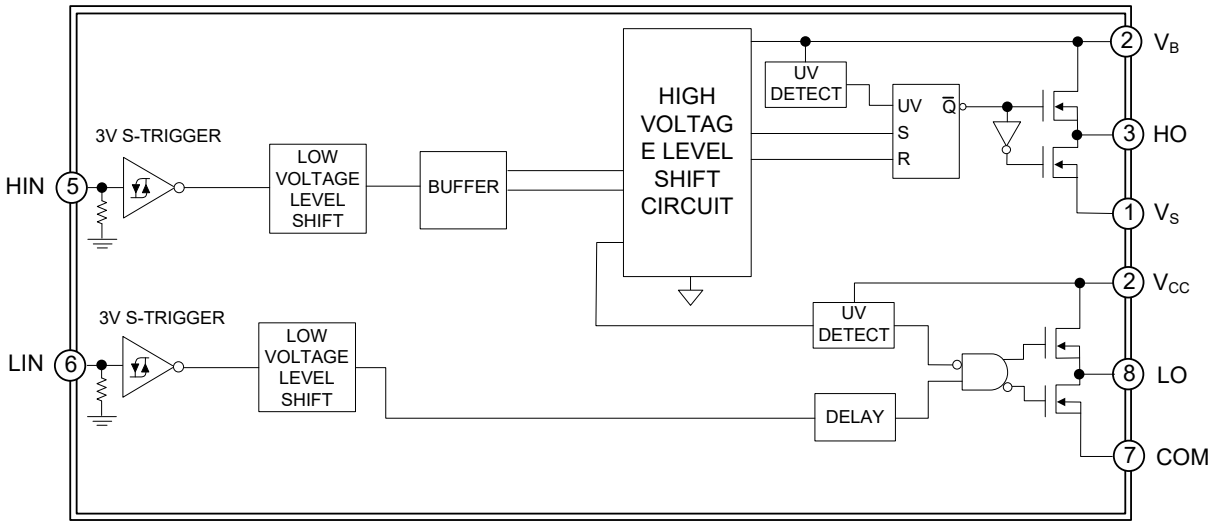
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{CC}	Low side supply
2	V_B	High side floating supply
3	HO	High side gate drive output
4	V_S	High side floating supply return
5	HIN	Logic input for high side gate driver outputs (HO), in phase
6	LIN	Logic input for low side gate driver outputs (LO), in phase
7	COM	Low side return
8	LO	Low side gate drive output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
High side floating supply voltage	V_B	-0.3 ~ 220	V
High side floating supply offset voltage	V_S	V_B - 20 ~ V_B + 0.3	V
High side floating output voltage	V_{HO}	V_S - 0.3 ~ V_B + 0.3	V
Low side fixed supply voltage	V_{CC}	-0.3 ~ 20	V
Low side output voltage	V_{LO}	-0.3 ~ V_{CC} + 0.3	V
Logic input voltage (HIN, LIN)	V_{IN}	-0.3 ~ V_{CC} + 0.3	V
Allowable offset supply voltage transient	dVs/dt	50	V/ns
Power Dissipation	P_D	0.625	W
Maximum Junction Temperature	T_J	+150	°C
Maximum Storage Temperature Range	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
High-Side Floating Absolute Voltage	V_B	V_S+10 ~ V_S+20	V
High-Side Floating Supply Offset Voltage	V_S	200 (Note)	V
High-Side Floating Output Voltage	V_{HO}	V_S ~ V_B	V
Low-Side and logic Fixed Supply Voltage	V_{CC}	10 ~ 20	V
Low-Side Output Voltage	V_{LO}	0 ~ V_{CC}	V
Logic Input Voltage (HIN &LIN)	V_{IN}	COM ~ V_{CC}	V
Ambient Temperature	T_A	-40 ~ +125	°C

Note: Logic operational for V_S of -5V to +200V. Logic state held for V_S of -5V to -V_{BS}.

■ THERMAL DATA

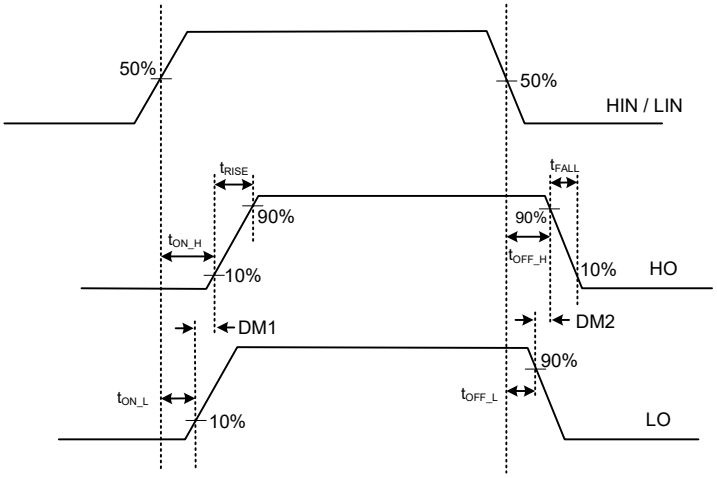
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	200	°C/W

■ ELECTRICAL CHARACTERISTICS

[V_{BIAS} (V_{CC}, V_{BS})=15V and T_A=25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Turn-ON Propagation Delay	t_{ON}	V_S=0V		60	100	ns
Turn-OFF Propagation Delay	t_{OFF}	V_S=200V		60	100	ns
Turn-ON Rise Time	t_r			25	40	ns
Turn-OFF Fall Time	t_f			15	35	ns
Turn-ON Delay matching (t_{ON_H}-t_{ON_L})	DM1				40	ns
Turn-OFF Delay matching (t_{OFF_H}-t_{OFF_L})	DM2				40	ns
Logic “1” Input Voltage	V_{IH}	V_{CC}=10V~20V	2.5			V
Logic “0” Input Voltage	V_{IL}	V_{CC}=10V~20V			0.7	V
High level Output Voltage, V_{BIAS} - V_O	V_{OH}	I_O=0A			1.4	V
Low Level Output Voltage, V_O	V_{OL}	I_O=2mA			0.1	V
Offset Supply Leakage Current	I_{LK}	V_B=V_S=200V			50	μA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{IN}=0V or 3.6V		120	210	μA
Quiescent V_{CC} Supply Current	I_{QCC}			300	300	μA
Logic “1” Input Bias Current	I_{IN+}	V_{IN}=3.6V		3	10	μA
Logic “0” Input Bias Current	I_{IN-}	V_{IN}=0V			5	μA
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}		8.3	9.0	9.7	V
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}		7.5	8.2	8.9	V
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}		8.3	9.0	9.7	V
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}		7.5	8.2	8.9	V
Output High Short Circuit Pulsed Current	I_{O+}	V_O=0V, P_W≤10μs		1		A
Output Low Short Circuit Pulsed Current	I_{O-}	V_O=15V, P_W≤10μs		1		A

■ AND WAVEFORMS



TIMING DIAGRAM

■ TYPICAL APPLICATION CIRCUIT