

**UT9P06M**

Preliminary

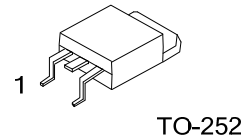
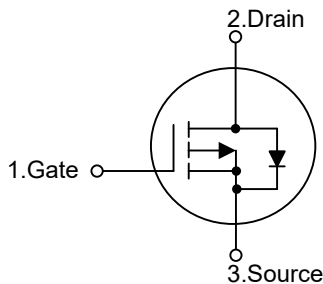
POWER MOSFET**-9.0A, -60V P-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **UT9P06M** is P-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with ideal for low voltage inverter applications.

The UTC **UT9P06M** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

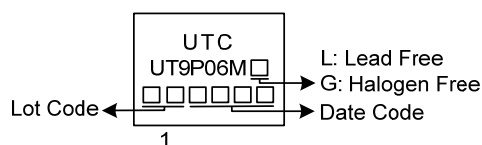
- * $R_{DS(ON)} \leq 180 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -4.5\text{A}$
- $R_{DS(ON)} \leq 240 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -4.5\text{A}$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT9P06ML-TN3-R	UT9P06MG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT9P06MG-TN3-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) TN3: TO-252
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

■ **ABSOLUTE MAXIMUM RATING** ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current ($T_C=25^{\circ}\text{C}$)	Continuous	I_D	-9	A
	Pulsed (Note 2)	I_{DM}	-18	A
Avalanche Energy (Note 3)	Single Pulsed (Note 3)	E_{AS}	11.5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.7	V/nS
Power Dissipation ($T_C=25^{\circ}\text{C}$)		P_D	28	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L = 0.1\text{mH}$, $I_{AS} = -15.2\text{A}$, $V_{DD} = -90\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq -9.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DS}$, $T_J \leq 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	4.46 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

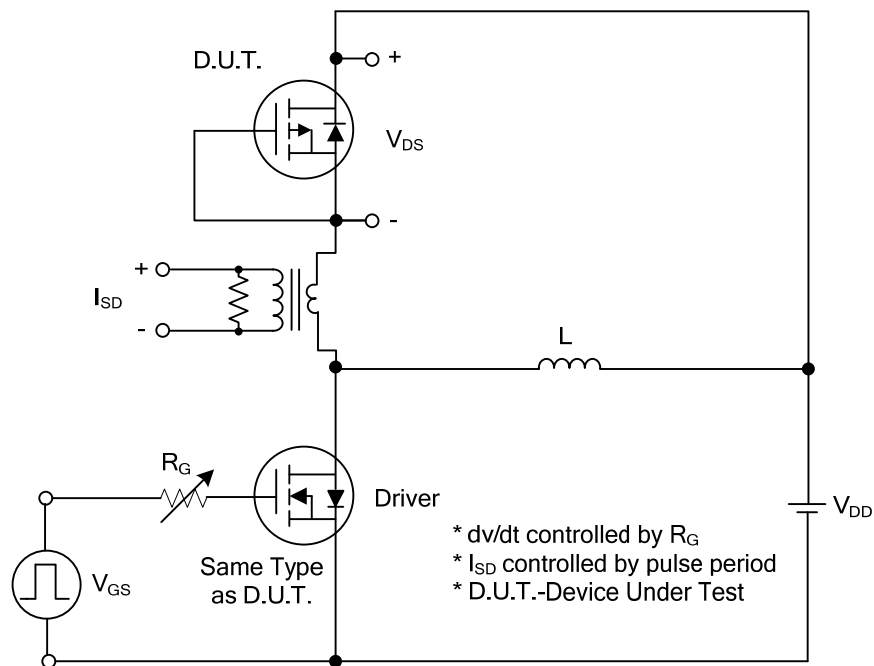
■ **ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =-250μA, V _{GS} =0V	-60			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-60V, V _{GS} =0V, T _J =25°C			-1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =-10V, I _D =-4.5A			180	mΩ
			V _{GS} =-4.5V, I _D =-4.5A			240	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz		422		pF
Output Capacitance		C _{OSS}			43		pF
Reverse Transfer Capacitance		C _{RSS}			31		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =-48V, V _{GS} =-10V, I _D =-9.0A (Note 1, 2)		6.8		nC
Gate to Source Charge		Q _{GS}			1.4		nC
Gate to Drain Charge		Q _{GD}			1.8		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =-30V, V _{GS} =-10V, I _D =-9.0A, R _G =25Ω (Note 1, 2)		3.5		ns
Rise Time		t _R			17		ns
Turn-off Delay Time		t _{D(OFF)}			36		ns
Fall-Time		t _F			23		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				-9	A
Maximum Body-Diode Pulsed Current		I _{SM}				-18	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =-9.0A, V _{GS} =0V			-1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =-9.0A, V _{GS} =0V,		60		ns
Reverse Recovery Charge		Q _{rr}	di _F /dt=100A/μs (Note 1)		55		ns

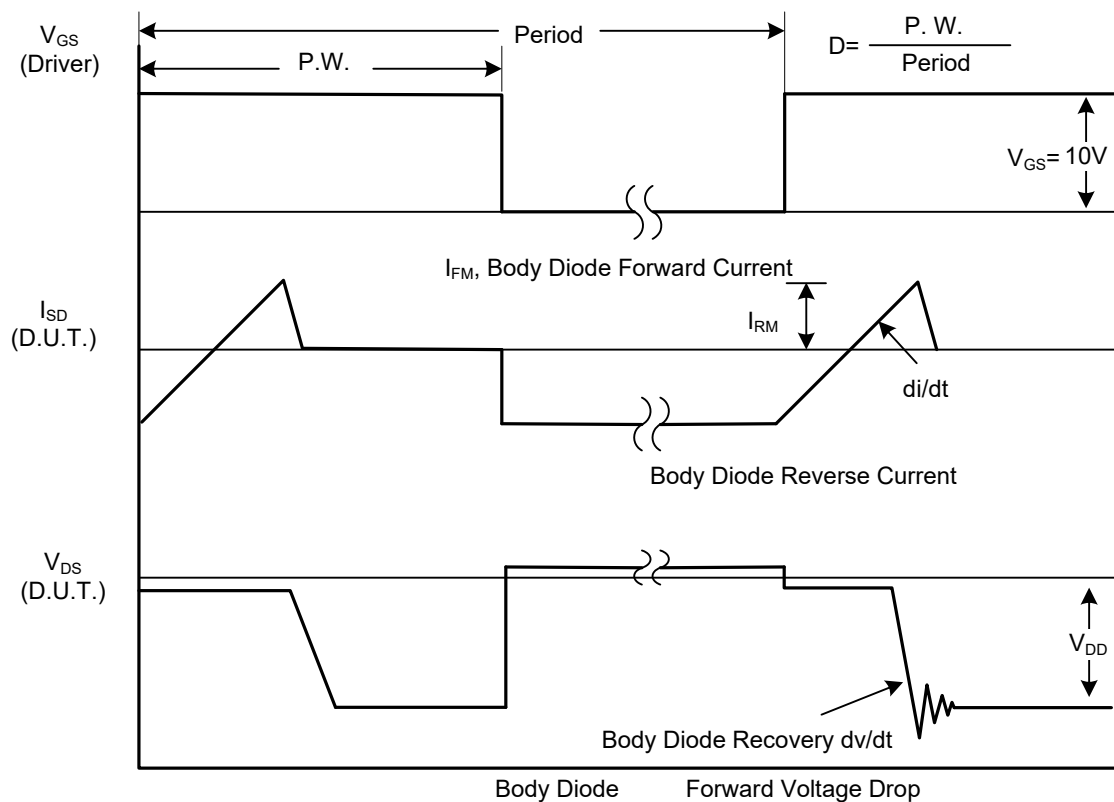
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

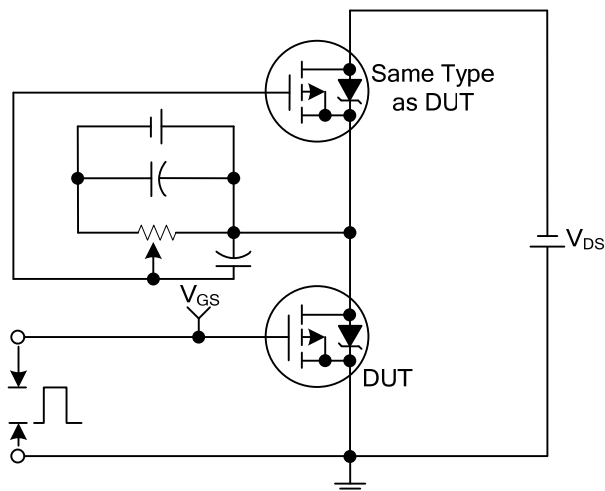


Peak Diode Recovery dv/dt Test Circuit

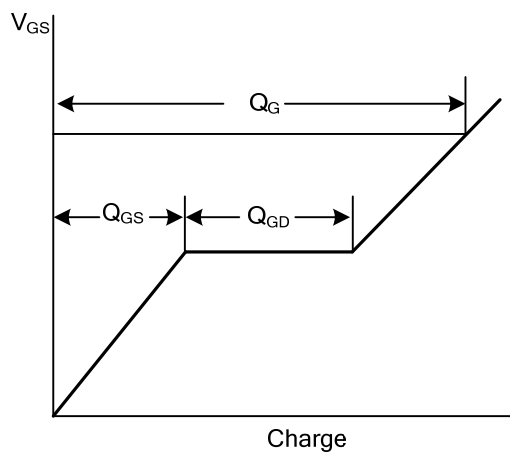


Peak Diode Recovery dv/dt Waveforms

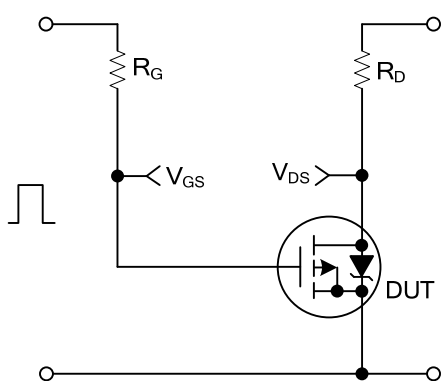
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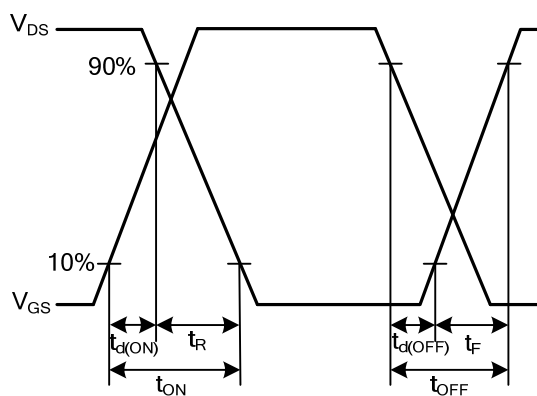
Gate Charge Test Circuit



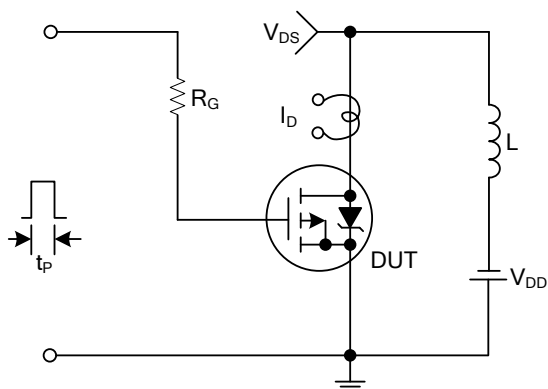
Gate Charge Waveforms



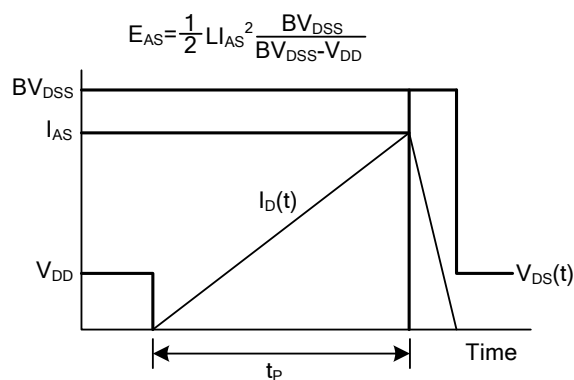
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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