



UT40N25H

Preliminary

POWER MOSFET

40A, 250V N-CHANNEL POWER MOSFET

DESCRIPTION

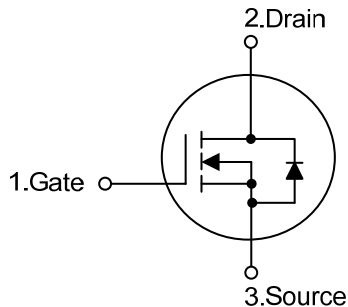
The UTC **UT40N25H** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance, low gate charge and high switching speed.

The UTC **UT40N25H** is suitable for high voltage synchronous rectifier and DC/DC converters, etc.

FEATURES

- * $R_{DS(ON)} \leq 62 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=20\text{A}$
- * High Switching Speed
- * High Cell Density Trench Technology

SYMBOL

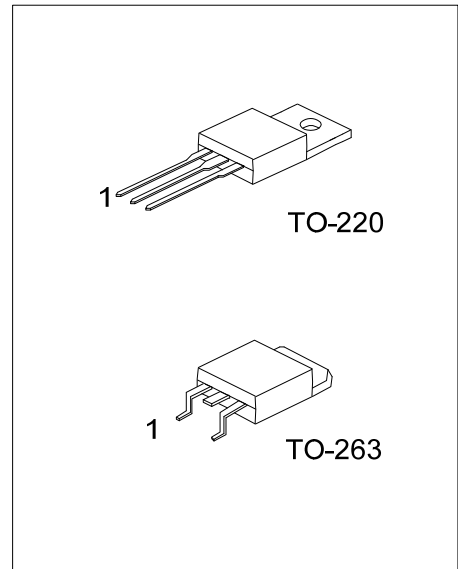


ORDERING INFORMATION

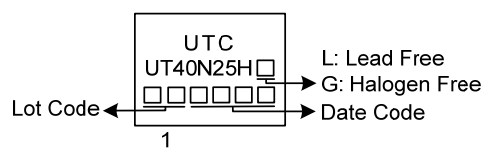
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT40N25HL-TA3-T	UT40N25HG-TA3-T	TO-220	G	D	S	Tube
UT40N25HL-TQ2-T	UT40N25HG-TQ2-T	TO-263	G	D	S	Tube
UT40N25HL-TQ2-R	UT40N25HG-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT40N25HG-TA3-T		(1)Packing Type	(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TQ2: TO-263 (3) G: Halogen Free and Lead Free, L: Lead Free
		(2)Package Type	
		(3)Green Package	



■ MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	250	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	40	A
	Pulsed (Note 2)	I_{DM}	120	A
Avalanche Energy (Note 3)	Single Pulsed (Note 3)	E_{AS}	5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.8	V/ns
Power Dissipation		P_D	120	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-40 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L=0.1\text{mH}$, $I_{AS}=10.6\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

4. $I_{SD}\leq 30\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case (Note)	θ_{JC}	1.04	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

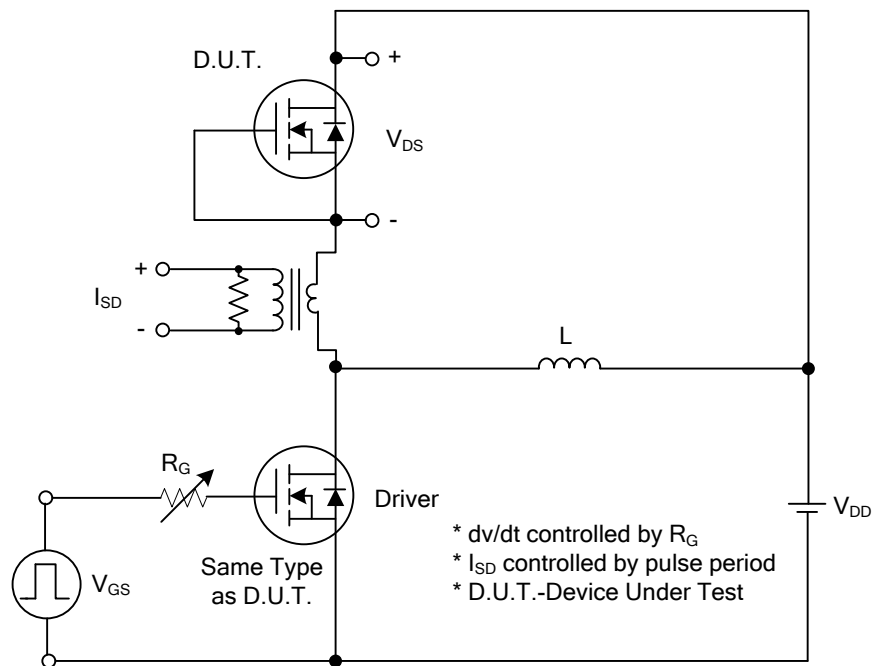
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	250			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =250V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A			62	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		9405		pF
Output Capacitance		C _{OSS}			290		pF
Reverse Transfer Capacitance		C _{RSS}			222		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =200V, V _{GS} =10V, I _D =40A (Note 1, 2)		190		nC
Gate to Source Charge		Q _{GS}			45		nC
Gate to Drain Charge		Q _{GD}			54		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =100V, V _{GS} =10V, I _D =40A, R _G =3Ω (Note 1, 2)		28		ns
Rise Time		t _R			20		ns
Turn-off Delay Time		t _{D(OFF)}			70		ns
Fall-Time		t _F			25		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				40	A
Maximum Body-Diode Pulsed Current		I _{SM}				120	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =40A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =30A, V _{GS} =0V,		150		ns
Reverse Recovery Charge		Q _{rr}	di _F /dt=100A/μs (Note 1)		0.92		μC

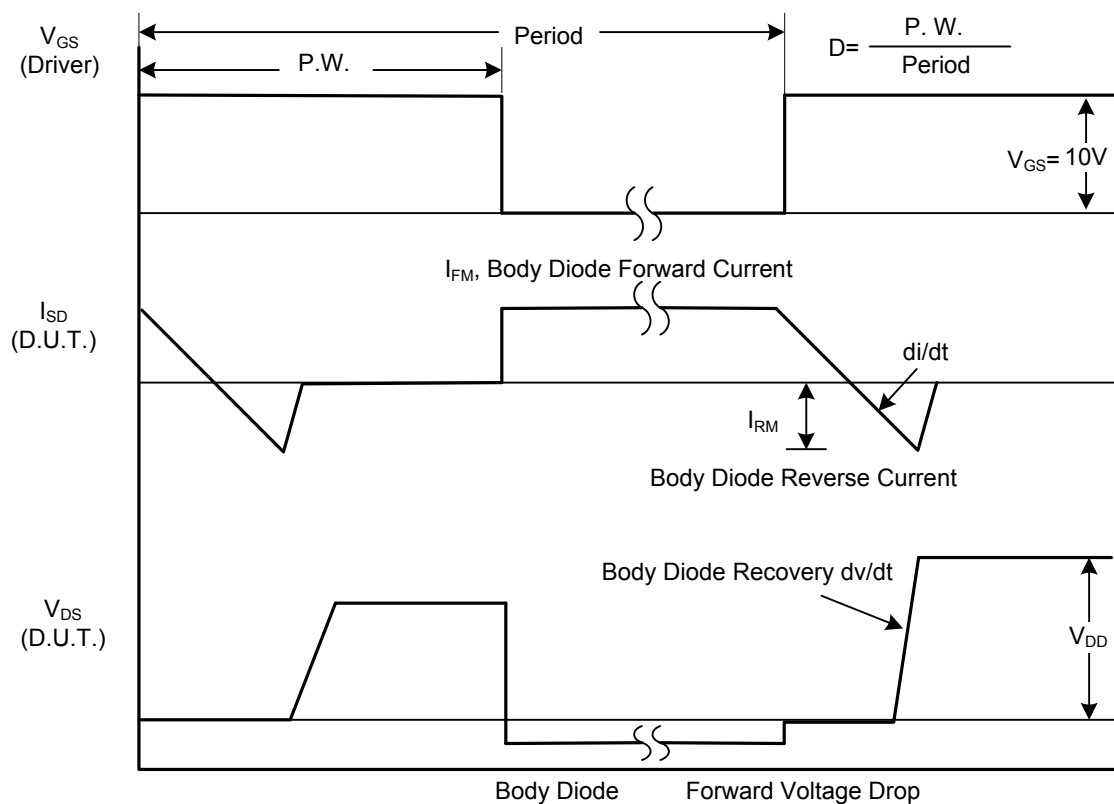
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

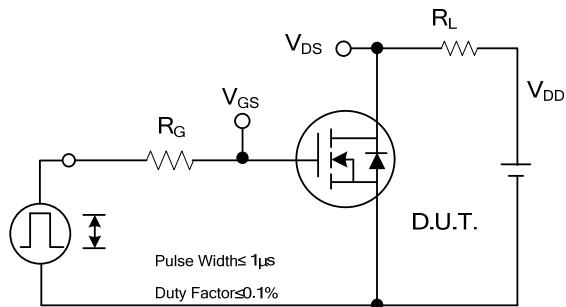


Peak Diode Recovery dv/dt Test Circuit

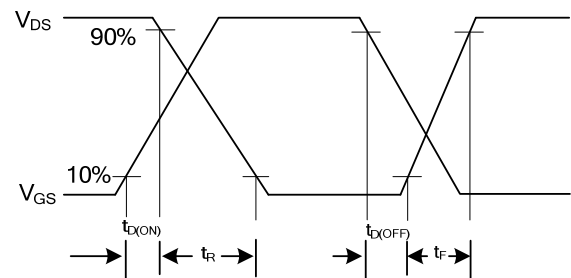


Peak Diode Recovery dv/dt Waveforms

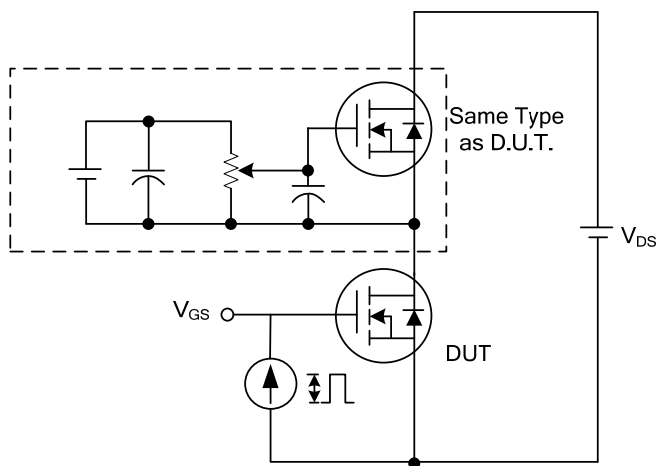
■ TEST CIRCUITS AND WAVEFORMS



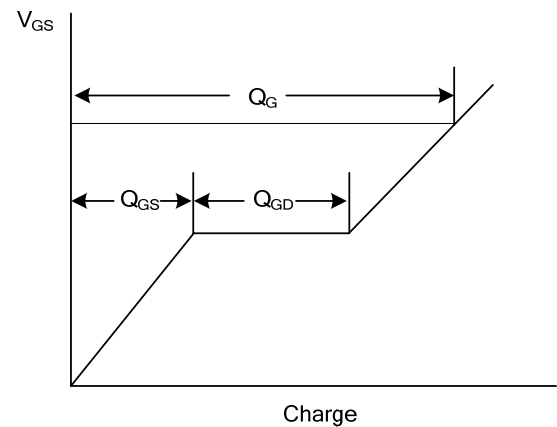
Switching Test Circuit



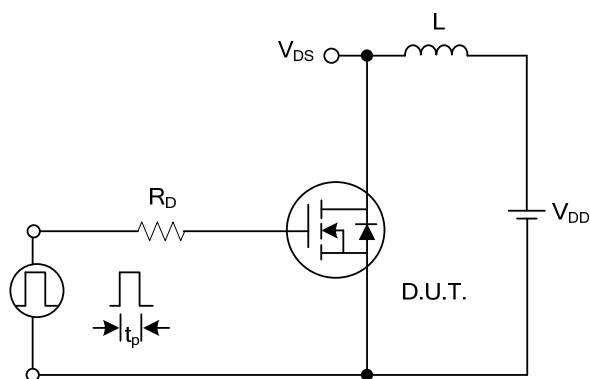
Switching Waveforms



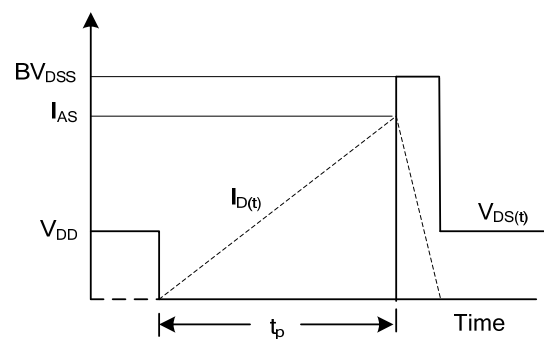
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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