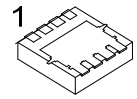
40A, 40V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET



PDFN3×3

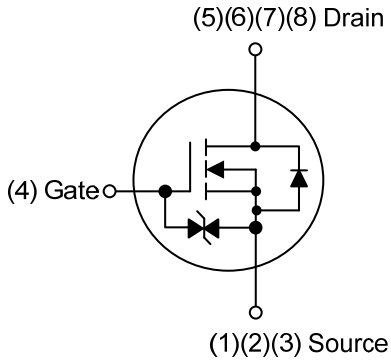
■ DESCRIPTION

The UTC **UT40N04HZ** is a N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

■ FEATURES

* $R_{DS(ON)} \leq 10\ m\Omega$ @ V_{GS}=10V, I_D=20A
* Low drain-source on-resistance
* Low leakage current?
* Enhancement mode
* With ESD Protected

■ SYMBOL



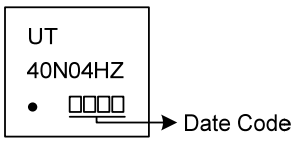
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT40N04HZL-P3030-R	UT40N04HZG-P3030-R	PDFN3×3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

UT40N04HZG-P3030-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P3030: PDFN3×3 (3) G: Halogen Free and Lead Free, K: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	40	A
	Pulsed (Note 2)	I_{DM}	80	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	60	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.9	V/ns
Power Dissipation		P_D	22	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L = 0.1mH, I_{AS} =34.6A, V_{DD} = 20V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤ 30A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, T_J ≤ T_{JMAX}, T_J = 25°C.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	75	°C/W
Junction to Case	θ_{JC}	5.68	°C/W

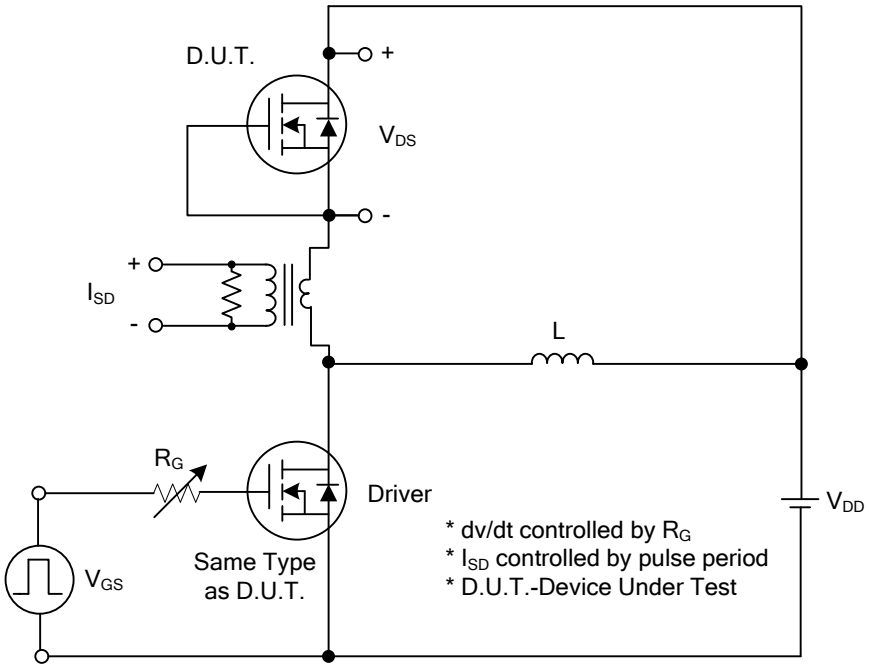
Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

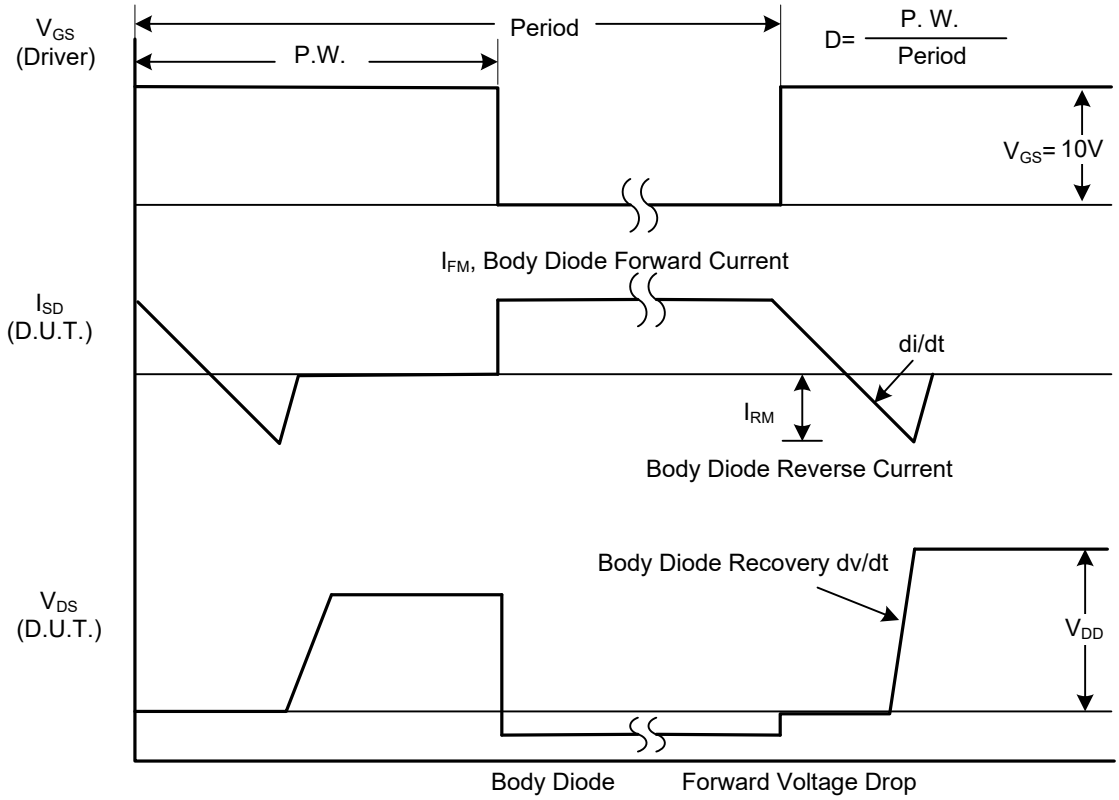
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	40			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=40V, V_{GS}=0V			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+10	μA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=20A			10	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz		1412		pF
Output Capacitance		C_{OSS}			184		pF
Reverse Transfer Capacitance		C_{RSS}			152		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{DS}=32V, V_{GS}=10V, I_D=40A		47		nC
Gate to Source Charge		Q_{GS}			5		nC
Gate to Drain Charge		Q_{GD}			20		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=20V, V_{GS}=10V, I_D=40A, R_G =3Ω		7		ns
Rise Time		t_R			17		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			130		ns
Fall-Time		t_F			71		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				40	A
Maximum Body-Diode Pulsed Current		I_{SM}				80	A
Drain-Source Diode Forward Voltage		V_{SD}	I_{SD}=40A			1.4	V
Body Diode Reverse Recovery Time		t_{rr}	I_S=30A, dI/dt=100A/μs		56		ns
Body Diode Reverse Recovery Charge		Q_{rr}			57		nC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

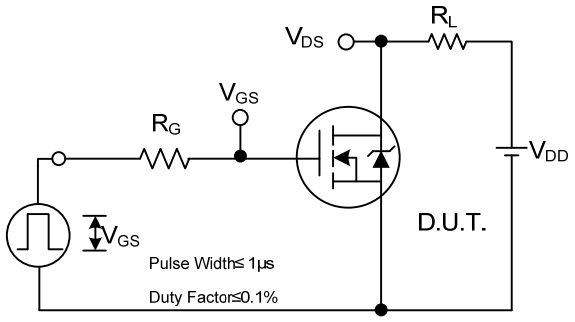


Peak Diode Recovery dv/dt Test Circuit

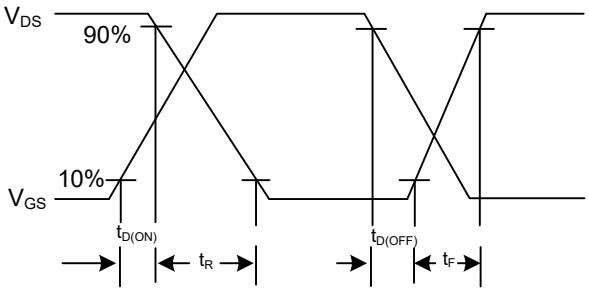


Peak Diode Recovery dv/dt Waveforms

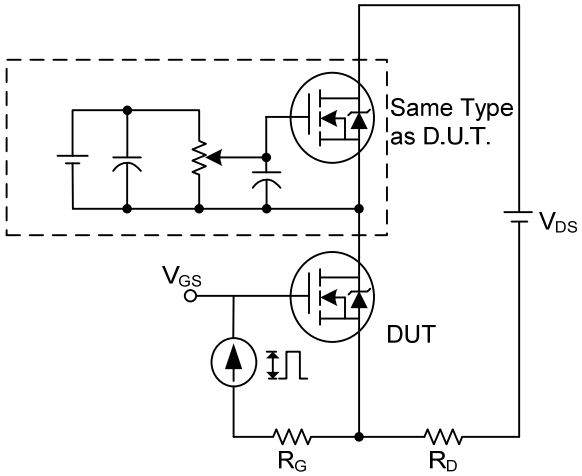
■ TEST CIRCUITS AND WAVEFORMS



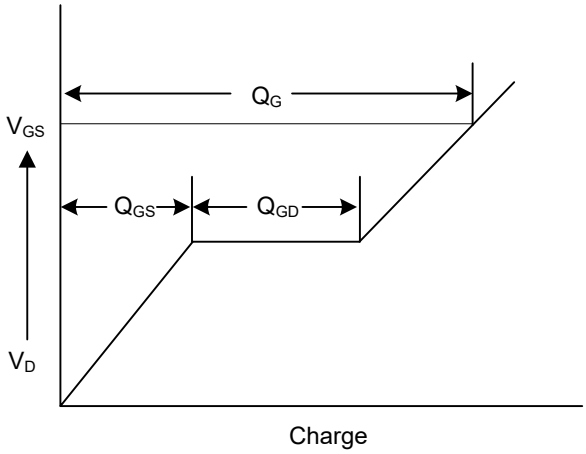
Switching Test Circuit



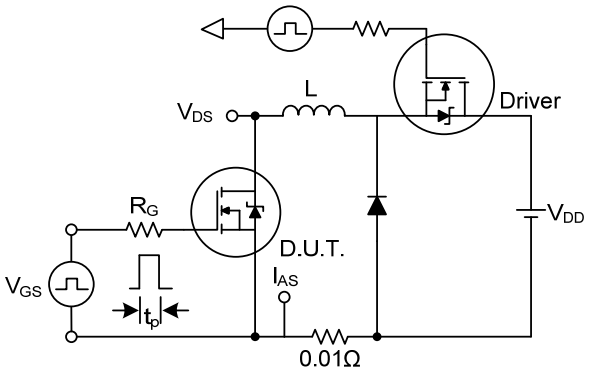
Switching Waveforms



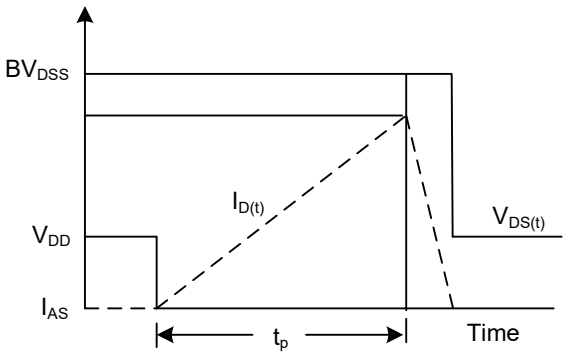
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms