

**UT25NP04**

Preliminary

Power MOSFET

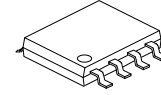
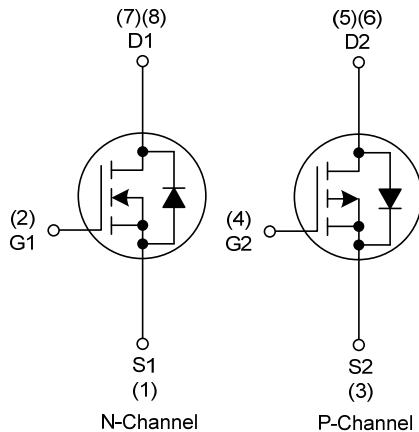
**DUAL ENHANCEMENT MODE
(N-CHANNEL / P-CHANNEL)****DESCRIPTION**

The UTC **UT25NP04** incorporates a N-channel MOSFET and a P-channel MOSFET, it uses UTC's advanced technology to provide customers a minimum on-state resistance, high switching speed, low gate charge and cost effectiveness.

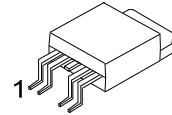
The UTC **UT25NP04** is universally applied in low voltage applications.

FEATURES***N-CHANNEL** $R_{DS(ON)} \leq 15\text{ m}\Omega @ V_{GS} = 10\text{V}, I_D = 6.0\text{A}$ $R_{DS(ON)} \leq 22\text{ m}\Omega @ V_{GS} = 4.5\text{V}, I_D = 5.0\text{A}$ ***P-CHANNEL** $R_{DS(ON)} \leq 40\text{ m}\Omega @ V_{GS} = -10\text{V}, I_D = -5.5\text{A}$ $R_{DS(ON)} \leq 55\text{ m}\Omega @ V_{GS} = -4.5\text{V}, I_D = -3.5\text{A}$

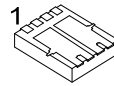
* High switching speed

SYMBOL

SOP-8



TO-252-4



PDFN5x6

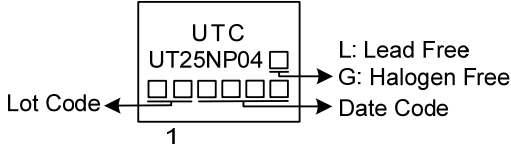
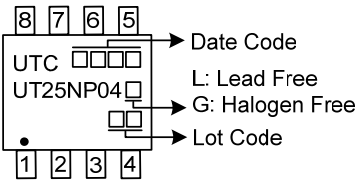
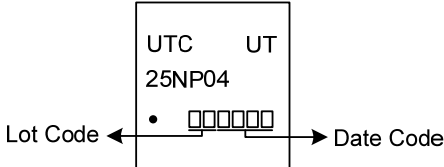
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT25NP04L-TN4-R	UT25NP04G-TN4-R	TO-252-4	S1	G1	D	S2	G2	-	-	-	Tape Reel
UT25NP04L-S08-R	UT25NP04G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel
UT25NP04L-P5060-R	UT25NP04G-P5060-R	PDFN5×6	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT25NP04G-TN4-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) TN4: TO-252-4, S08: SOP-8, P5060: PDFN5×6 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

PACKAGE	MARKING
TO-252-4	 UTC UT25NP04 Lot Code Date Code L: Lead Free G: Halogen Free
SOP-8	 UTC UT25NP04 Lot Code Date Code L: Lead Free G: Halogen Free
PDFN5×6	 UTC UT 25NP04 Lot Code Date Code

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS		UNIT
			N-CHANNEL	P-CHANNEL	
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Drain Current	Continuous	I_D	12	-12	A
	Pulsed (Note 1)	I_{DM}	36	-36	A
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	3.5	40	mJ
Power Dissipation	TO-252-4	P_D	50		W
	SOP-8		1.9		W
	PDFN5x6		28		W
Junction Temperature		T_J	$-55 \sim +150$		$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	$-55 \sim +150$		$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. N-Channel: $L = 0.1\text{mH}$, $I_{AS} = 8.4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

P-Channel: $L = 0.1\text{mH}$, $I_{AS} = -28.3\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252-4	θ_{JA}	110	$^{\circ}\text{C/W}$
	SOP-8		125	$^{\circ}\text{C/W}$
	PDFN5x6		65	$^{\circ}\text{C/W}$
Junction to Case	TO-252-4	θ_{JC}	2.5	$^{\circ}\text{C/W}$
	SOP-8		65.7	$^{\circ}\text{C/W}$
	PDFN5x6		4.46	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^\circ\text{C}$, unless otherwise specified)

N-Channel

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance (Note 2)		R _{DS(ON)}	V _{GS} =10V, I _D =6.0A			15	mΩ
			V _{GS} =4.5V, I _D =5.0A			22	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		972		pF
Output Capacitance		C _{OSS}			114		pF
Reverse Transfer Capacitance		C _{RSS}			98		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 2)		Q _G	V _{GS} =10V, V _{DS} =32V, I _D =25A		37		nC
Gate to Source Charge		Q _{GS}			4		nC
Gate to Drain Charge		Q _{GD}			14		nC
Turn-ON Delay Time (Note 2)		t _{D(ON)}	V _{DS} =20V, V _{GS} =10V, I _D =25A, R _G =3Ω		8		ns
Rise Time		t _R			16		ns
Turn-OFF Delay Time		t _{D(OFF)}			28		ns
Fall-Time		t _F			19		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage(Note 2)		V _{SD}	I _S =25A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =25A, V _{GS} =0V,		11.2		nS
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs		2.8		nC

■ ELECTRICAL CHARACTERISTICS (Cont.)

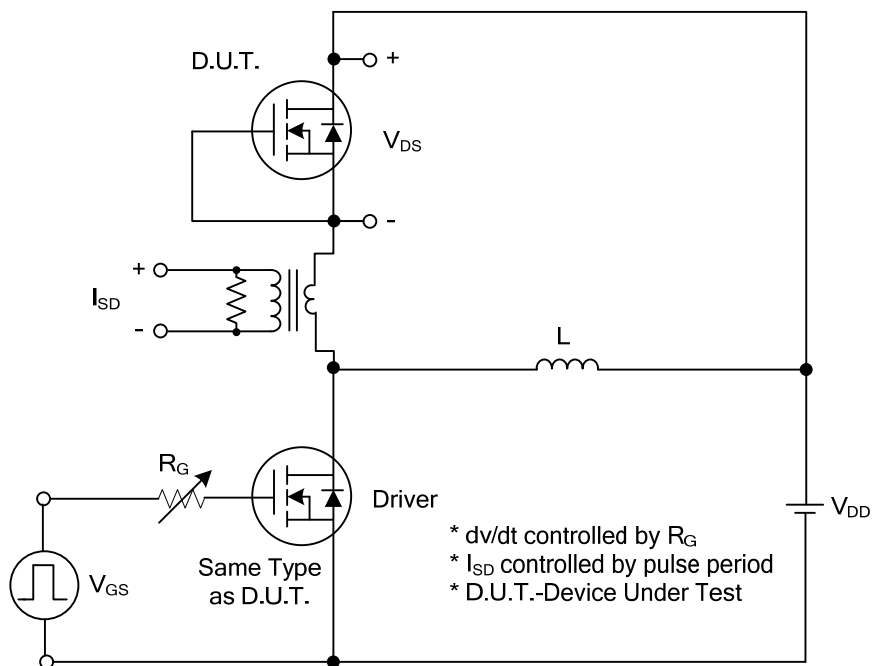
P-Channel

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =-250μA, V _{GS} =0V	-40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-40V, V _{GS} =0V			-1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance (Note 2)		R _{DS(ON)}	V _{GS} =-10V, I _D =-5.5A			40	mΩ
			V _{GS} =-4.5V, I _D =-3.5A			55	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz		1266		pF
Output Capacitance		C _{OSS}			134		pF
Reverse Transfer Capacitance		C _{RSS}			107		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 2)		Q _G	V _{GS} =-10V, V _{DS} =-32V, I _D =-25A		27		nC
Gate to Source Charge		Q _{GS}			9		nC
Gate to Drain Charge		Q _{GD}			9		nC
Turn-ON Delay Time (Note 2)		t _{D(ON)}	V _{DS} =-20V, V _{GS} =-10V, I _D =-25A, R _G =3Ω		7		ns
Rise Time		t _R			16		ns
Turn-OFF Delay Time		t _{D(OFF)}			49		ns
Fall-Time		t _F			26		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage(Note 2)		V _{SD}	I _S =-25A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =-25A, V _{GS} =0V,		53		nS
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs		44		nC

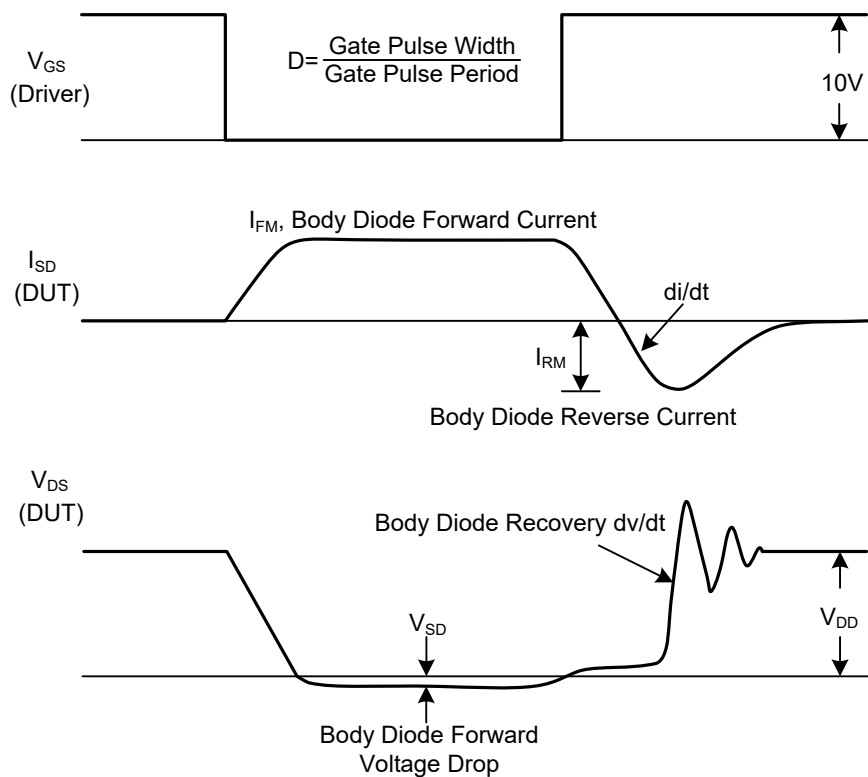
Notes: 1. Pulse width limited by maximum junction temperature

2. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

■ TEST CIRCUITS AND WAVEFORMS



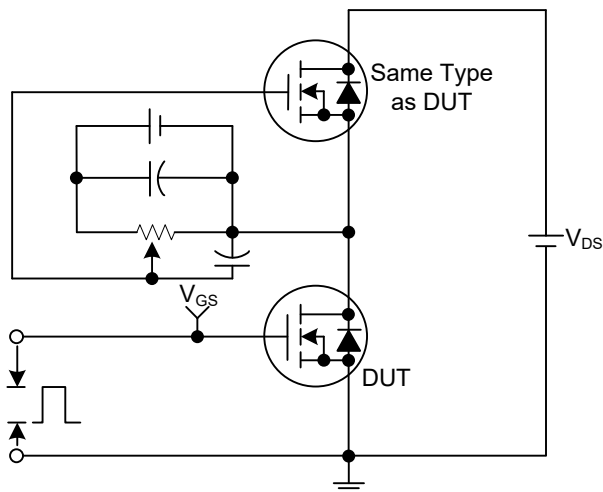
Peak Diode Recovery dv/dt Test Circuit



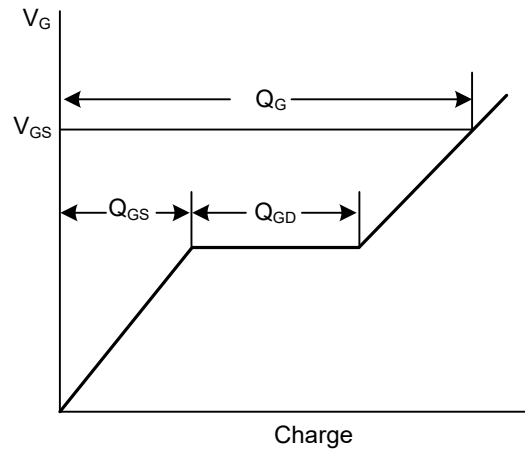
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

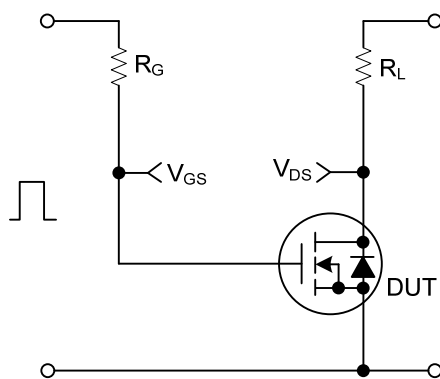
N-CHANNEL



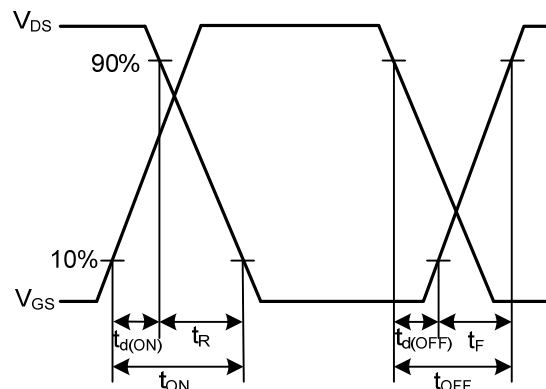
Gate Charge Test Circuit



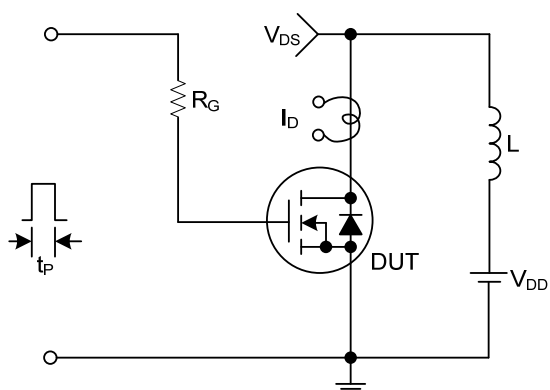
Gate Charge Waveforms



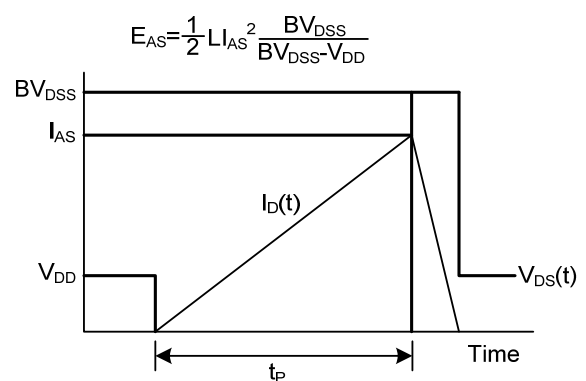
Resistive Switching Test Circuit



Resistive Switching Waveforms



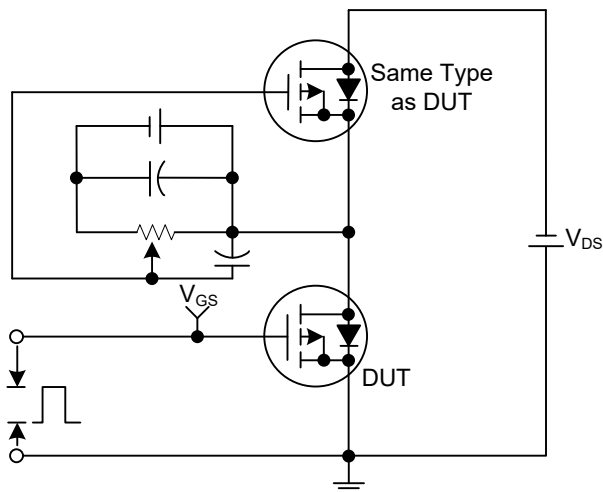
Unclamped Inductive Switching Test Circuit



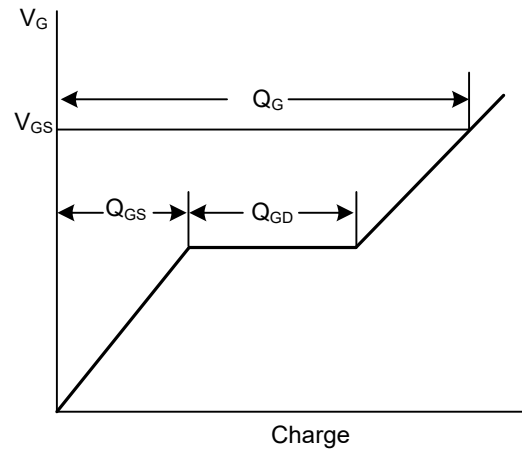
Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS

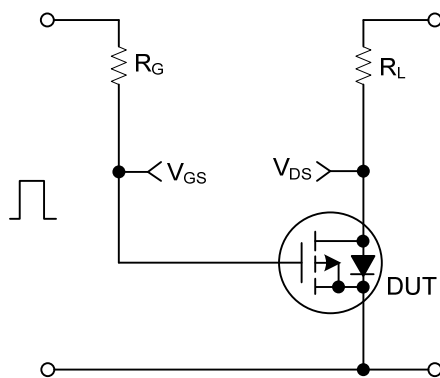
P-CHANNEL



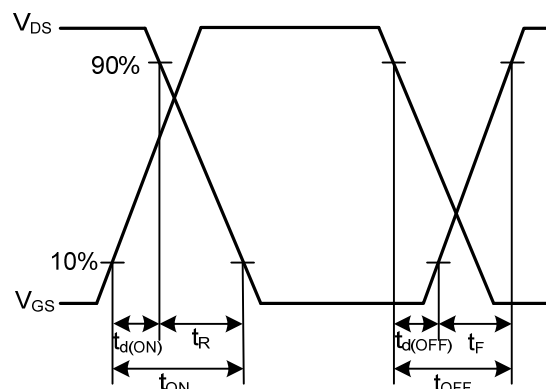
Gate Charge Test Circuit



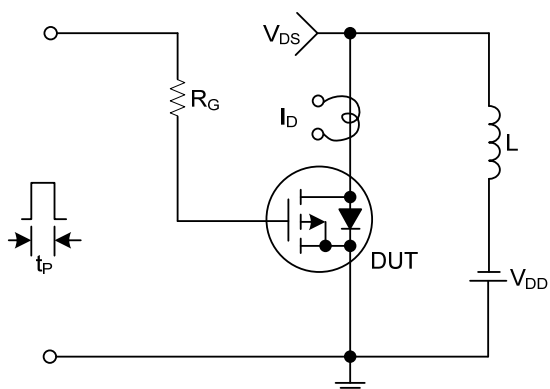
Gate Charge Waveforms



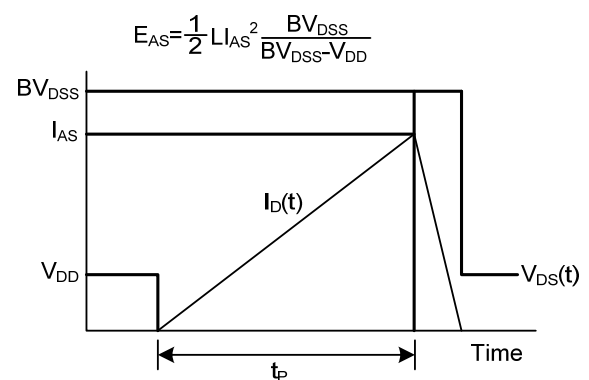
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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