

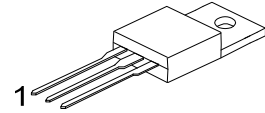
**UT200N04**

Preliminary

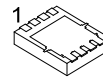
POWER MOSFET**200A, 40V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **UT200N04** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

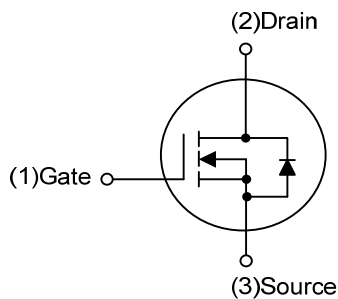
The UTC **UT200N04** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES*** TO-220**
 $R_{DS(ON)} \leq 2.5 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=50\text{A}$
 $R_{DS(ON)} \leq 3.3 \text{ m}\Omega @ V_{GS}=4.5\text{V}, I_D=50\text{A}$
*** PDFN5×6**
 $R_{DS(ON)} \leq 2.5 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=50\text{A}$
 $R_{DS(ON)} \leq 3.3 \text{ m}\Omega @ V_{GS}=4.5\text{V}, I_D=50\text{A}$
*** High Switching Speed**

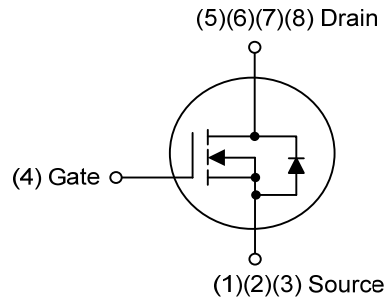
TO-220



PDFN5×6

SYMBOL

TO-220



PDFN5×6

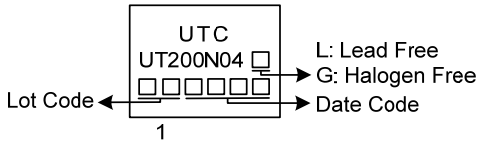
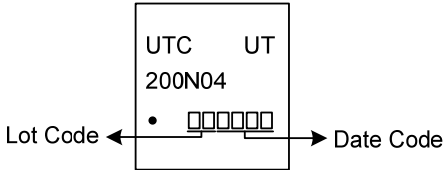
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT200N04L-TA3-T	UT200N04G-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
UT200N04L-P5060-R	UT200N04G-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT200N04G-TA3-T 		(1)Packing Type	(1) T: Tube, R: Tape Reel
		(2)Package Type	(2) TA3: TO-220, P5060: PDFN5×6
		(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

TO-220	PDFN5×6
 Diagram of TO-220 marking: A rectangular package with 'UTC' and 'UT200N04' printed on top. Below the part number is a small square symbol. To the left of the package is 'Lot Code' with an arrow pointing to a series of five squares. To the right is 'Date Code' with an arrow pointing to a series of four squares. Below the package is a small square symbol with the number '1' below it. UTC UT200N04 Lot Code → [] [] [] [] [] → Date Code 1 L: Lead Free G: Halogen Free	 Diagram of PDFN5×6 marking: A rectangular package with 'UTC' and 'UT 200N04' printed on top. Below the part number is a small square symbol. To the left of the package is 'Lot Code' with an arrow pointing to a series of five squares. To the right is 'Date Code' with an arrow pointing to a series of four squares. UTC UT 200N04 Lot Code → [] [] [] [] [] → Date Code

■ **ABSOLUTE MAXIMUM RATING** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	± 12	V
Drain Current	Continuous	I_D	200	A
	Pulsed (Note 2)	I_{DM}	400	A
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.5	V/ns
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	423	mJ
Power Dissipation	TO-220	P_D	150	W
	PDFN5×6		110	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-20 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
 3. $L = 0.1\text{mH}$, $I_{AS} = 92\text{A}$, $V_{DD} = 10\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^{\circ}\text{C/W}$
	PDFN5×6		65(Note)	$^{\circ}\text{C/W}$
Junction to Case	TO-220	θ_{JC}	0.83	$^{\circ}\text{C/W}$
	PDFN5×6		1.13(Note)	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

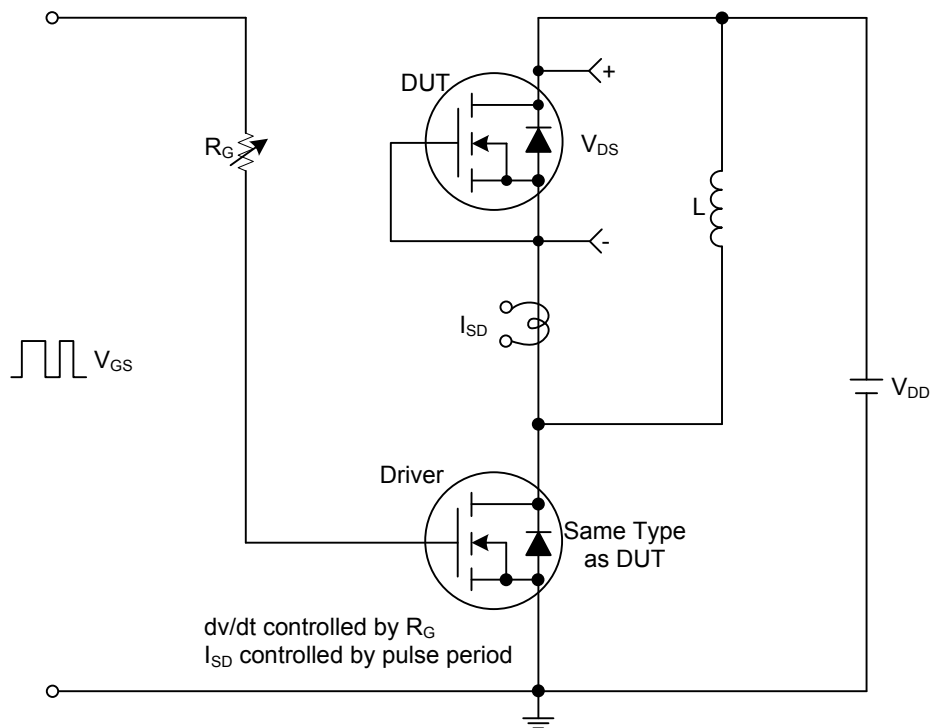
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+12V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-12V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	TO-220	R _{DS(ON)}	V _{GS} =10V, I _D =50A			2.5	mΩ
			V _{GS} =4.5V, I _D =50A			3.3	mΩ
	PDFN5×6		V _{GS} =10V, I _D =50A			2.5	mΩ
			V _{GS} =4.5V, I _D =50A			3.3	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		8800		pF
Output Capacitance		C _{OSS}			916		pF
Reverse Transfer Capacitance		C _{RSS}			805		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =32V, V _{GS} =4.5V, I _D =200A (Note 1, 2)		120		nC
Gate to Source Charge		Q _{GS}			40		nC
Gate to Drain Charge		Q _{GD}			65		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DD} =20V, V _{GS} =10V, I _D =200A, R _G =3.3Ω (Note 1, 2)		14		ns
Rise Time		t _R			26		ns
Turn-off Delay Time		t _{D(OFF)}			250		ns
Fall-Time		t _F			115		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				200	A
Maximum Body-Diode Pulsed Current		I _{SM}				400	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =200A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)		t _{rr}	I _S =30A, V _{GS} =0V,		70		nS
Reverse Recovery Charge		Q _{rr}	dl _F /dt =100A/μs		115		nC

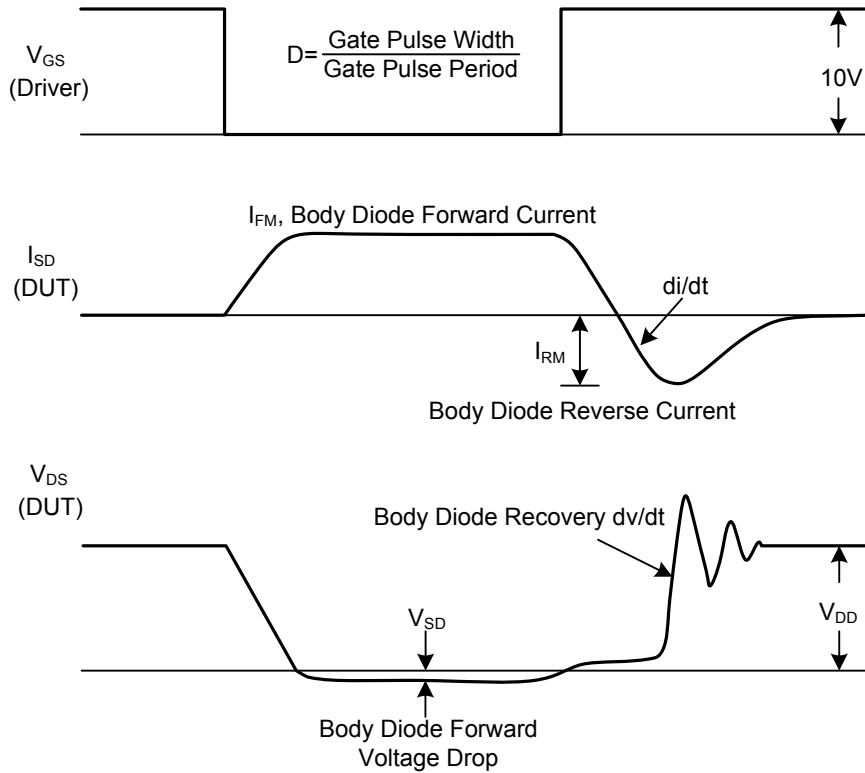
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



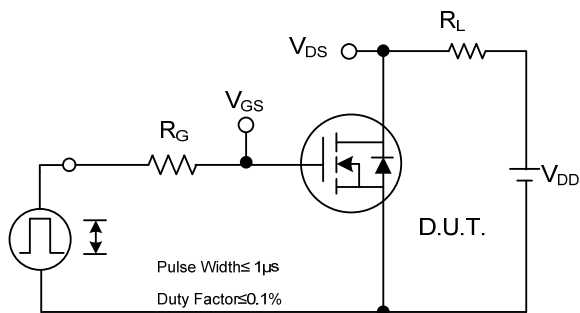
Peak Diode Recovery dv/dt Test Circuit



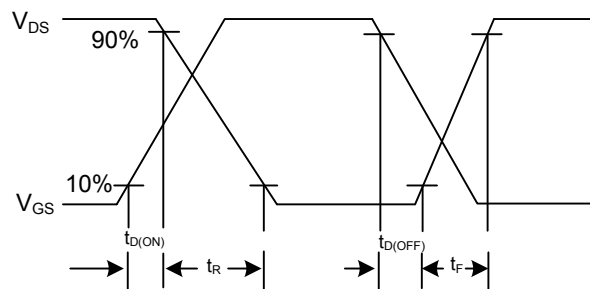
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

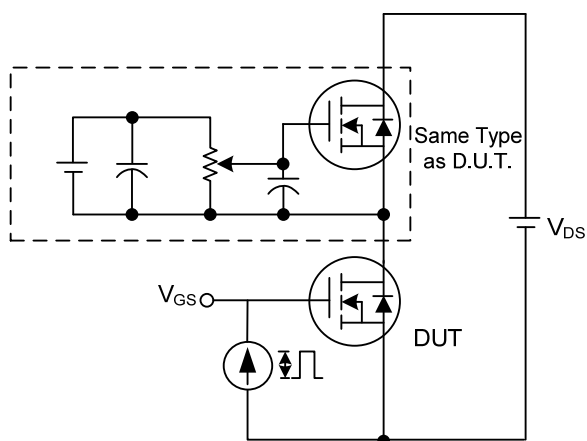
■ TEST CIRCUITS AND WAVEFORMS



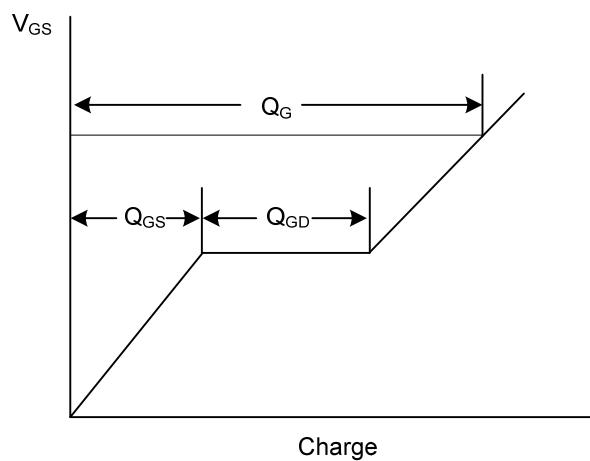
Switching Test Circuit



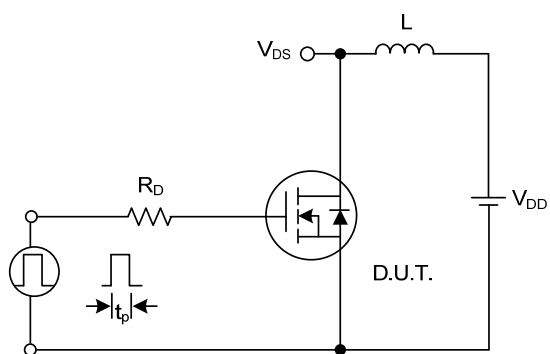
Switching Waveforms



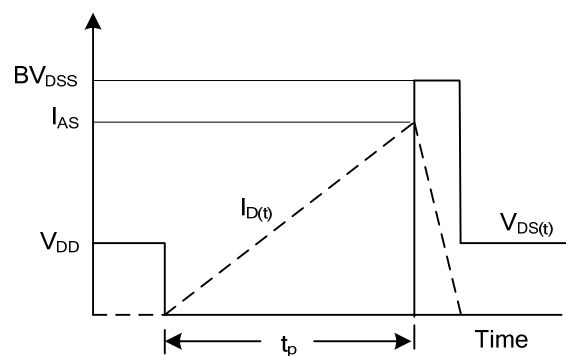
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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