



UT120N10H

Preliminary

Power MOSFET

120A, 100V N-CHANNEL POWER MOSFET

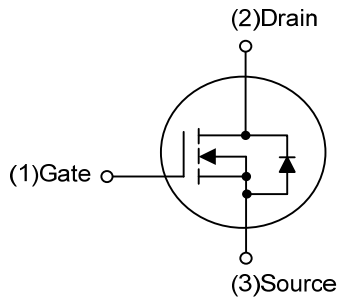
DESCRIPTION

The UTC **UT120N10H** is a N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

FEATURES

- * $R_{DS(ON)} \leq 8.5 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=60\text{A}$
- * Improved dv/dt capability
- * High Switching Speed
- * Fast switching

SYMBOL

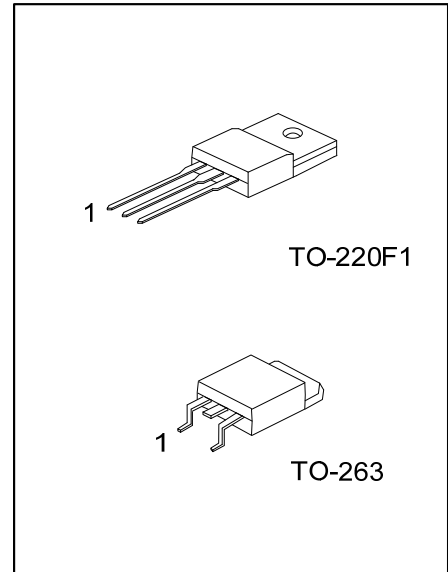


ORDERING INFORMATION

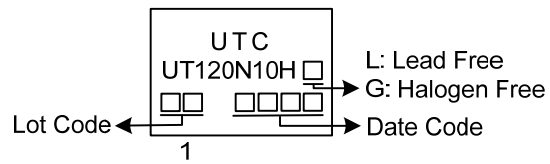
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT120N10HL-TF1-T	UT120N10HG-TF1-T	TO-220F1	G	D	S	Tube
UT120N10HL-TQ2-T	UT120N10HG-TQ2-T	TO-263	G	D	S	Tube
UT120N10HL-TQ2-R	UT120N10HG-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT120N10HG-TF1-T		(1) Packing Type	(1) T: Tube, R: Tape Reel
		(2) Package Type	(2) TF1: TO-220F1, TQ2: TO-263
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	120	A
	Pulsed	I_{DM}	240	A
Avalanche Energy	Single Pulsed	E_{AS}	194	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	9.3	V/ns
Power Dissipation	TO-263	P_D	215	W
	TO-220F1		49	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 62.2\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-263	θ_{JC}	0.58	$^{\circ}\text{C}/\text{W}$
	TO-220F1		2.55	$^{\circ}\text{C}/\text{W}$

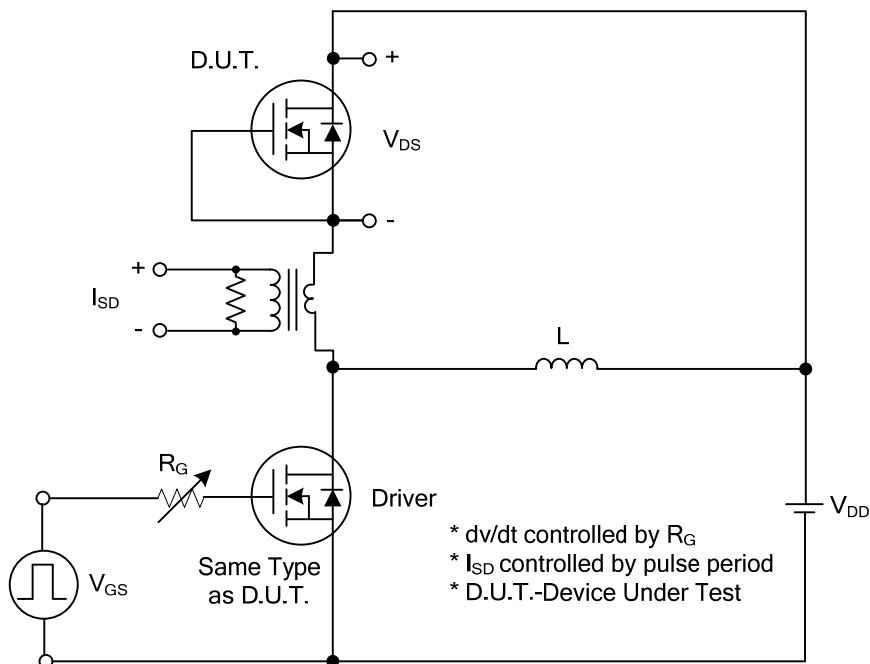
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	100			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	I _D =250μA, V _{DS} =V _{GS}	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =60A			8.5	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1MHz		1.4		nF
Output Capacitance		C _{OSS}			724		pF
Reverse Transfer Capacitance		C _{RSS}			441		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DD} =80V, V _{GS} =10V, I _D =120A, (Note 1, 2)		240		nC
Gate to Source Charge		Q _{GS}			57		nC
Gate to Drain Charge		Q _{GD}			20		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =40V, V _{GS} =10V I _D =120A, R _G =3Ω (Note 1, 2)		41		ns
Rise Time		t _R			30		ns
Turn-OFF Delay Time		t _{D(OFF)}			90		ns
Fall-Time		t _F			47		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				120	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =120A			1.4	V
Reverse Recovery Time		t _{rr}	I _S =30A, V _{GS} =0V		138		nS
Reverse Recovery Charge (Note 1)		Q _{rr}	dI _F /dt=100A/μs		223		nC

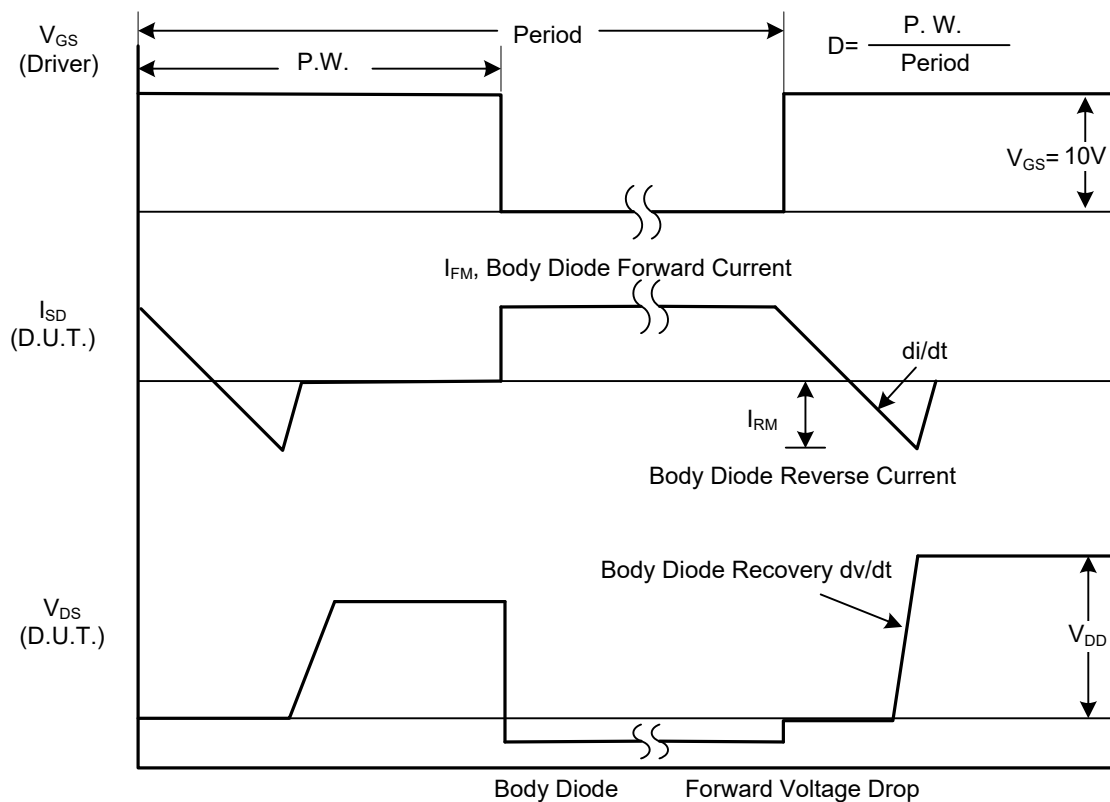
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS

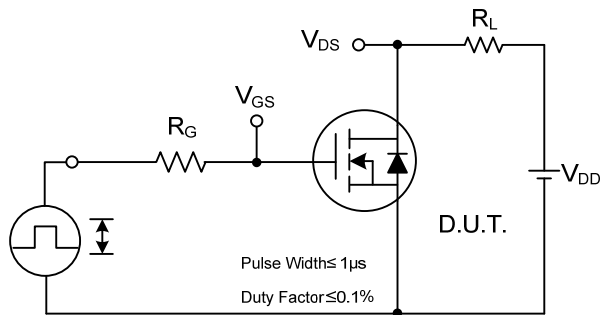


Peak Diode Recovery dv/dt Test Circuit

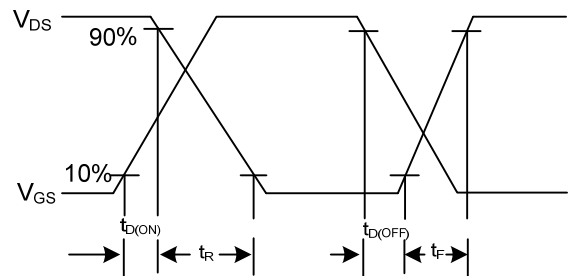


Peak Diode Recovery dv/dt Waveforms

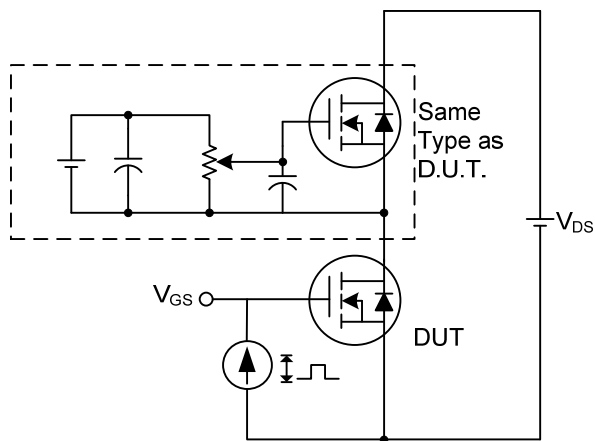
■ TEST CIRCUITS AND WAVEFORMS



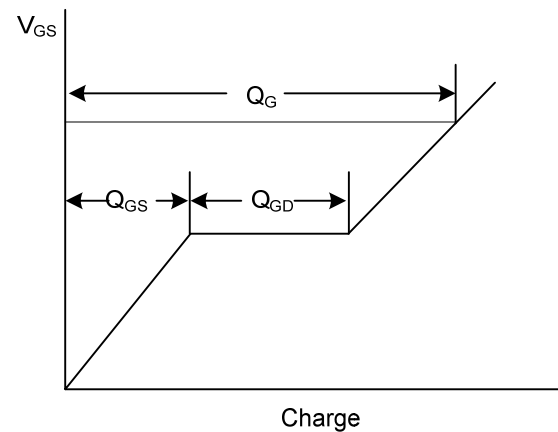
Switching Test Circuit



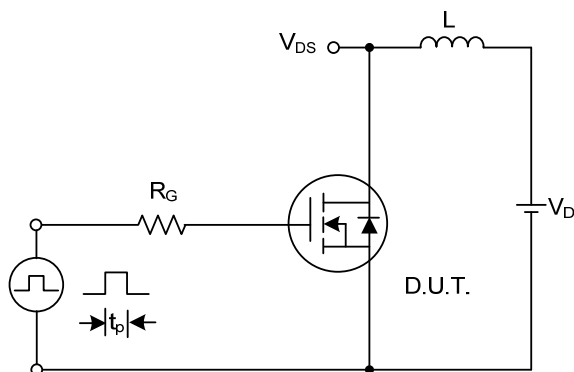
Switching Waveforms



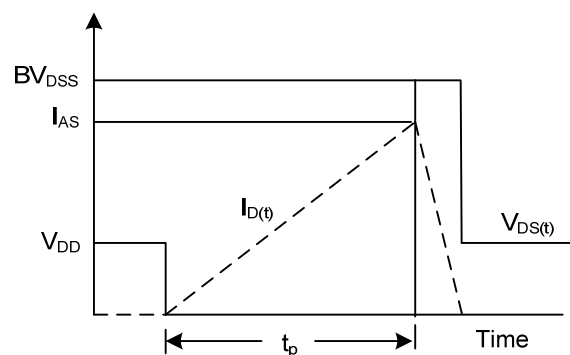
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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