

**UT100N10H**

Preliminary

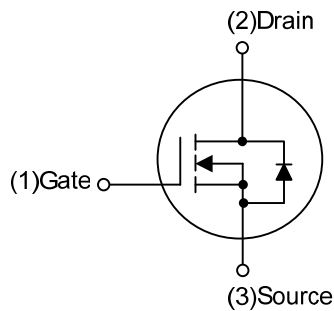
Power MOSFET

**100A, 100V N-CHANNEL
POWER MOSFET****DESCRIPTION**

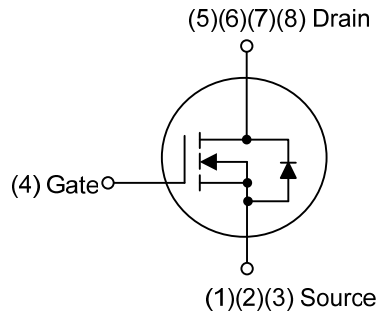
The UTC **UT100N10H** is an N-channel enhancement mode Power FET, it uses UTC's advanced technology to provide customers a minimum on-state resistance and high switching speed.

FEATURES

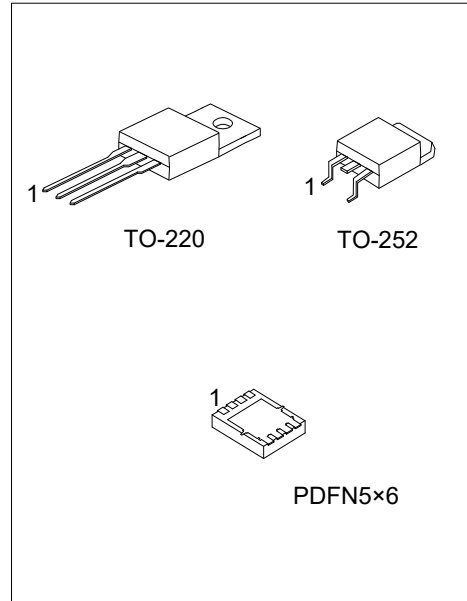
- * $R_{DS(ON)} \leq 12.5 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=50\text{A}$
- * High switching speed
- * Improved dv/dt capability

SYMBOL

TO-220 / TO-252



PDFN5×6

**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT100N10HL-TA3-T	UT100N10HG-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
UT100N10HL-TN3-R	UT100N10HG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT100N10HL-P5060-R	UT100N10HG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT100N10HG-TA3-T		(1) Packing Type	(1) T: Tube, R: Tape Reel
		(2) Package Type	(2) TA3: TO-220, TN3: TO-252, P5060: PDFN5×6
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

TO-220 / TO-252	PDFN5×6
UTC UT100N10H□ □□□□□□ Lot Code ← 1 L: Lead Free G: Halogen Free → Date Code	UTC UT 100N10H • □□□□□□ Lot Code ← → Date Code

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	100	V
Gate-Source Voltage		V _{GSS}	±20	V
Drain Current	Continuous	I _D	100	A
	Pulsed	I _{DM}	200	A
Avalanche Energy	Single Pulsed	E _{AS}	81	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.1	V/ns
Power Dissipation	TO-220	P _D	125	W
	TO-252		54	W
	PDFN5×6		40	W
Junction Temperature		T _J	+150	°C
Storage Temperature Range		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L = 0.1mH, I_{AS} = 40A, V_{DD} = 30V, R_G = 25Ω, Starting T_J = 25°C

4. I_{SD} ≤ 30A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ _{JA}	62.5	°C/W
	TO-252		110	°C/W
	PDFN5×6		65 (Note)	°C/W
Junction to Case	TO-220	θ _{JC}	1	°C/W
	TO-252		2.31 (Note)	°C/W
	PDFN5×6		3.125 (Note)	°C/W

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

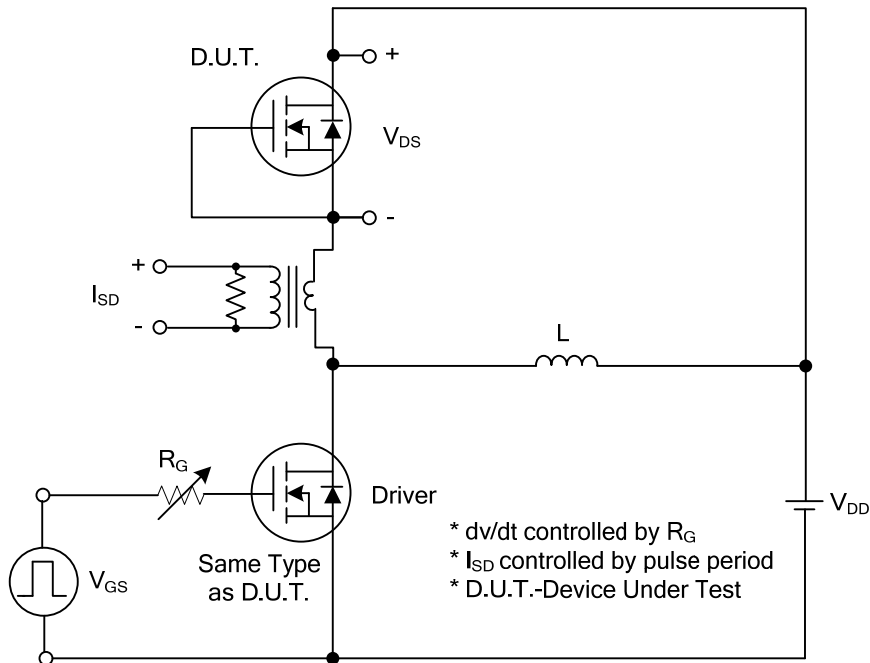
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	100			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	I _D =250μA, V _{DS} =V _{GS}	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =50A			12.5	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1MHz		4226		pF
Output Capacitance		C _{OSS}			376		pF
Reverse Transfer Capacitance		C _{RSS}			283		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DD} =80V, V _{GS} =10V, I _D =100A, (Note 1, 2)		100		nC
Gate to Source Charge		Q _{GS}			27		nC
Gate to Drain Charge		Q _{GD}			25		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =50V, V _{GS} =10V I _D =100A, R _G =3Ω (Note 1, 2)		20		ns
Rise Time		t _R			21		ns
Turn-OFF Delay Time		t _{D(OFF)}			44		ns
Fall-Time		t _F			24		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				100	A
Maximum Body-Diode Pulsed Current		I _{SM}				200	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =100A			1.4	V
Reverse Recovery Time		t _{rr}	I _S =30A, V _{GS} =0V		138		nS
Reverse Recovery Charge (Note 1)		Q _{rr}	dI _F /dt=100A/μs		341		nC

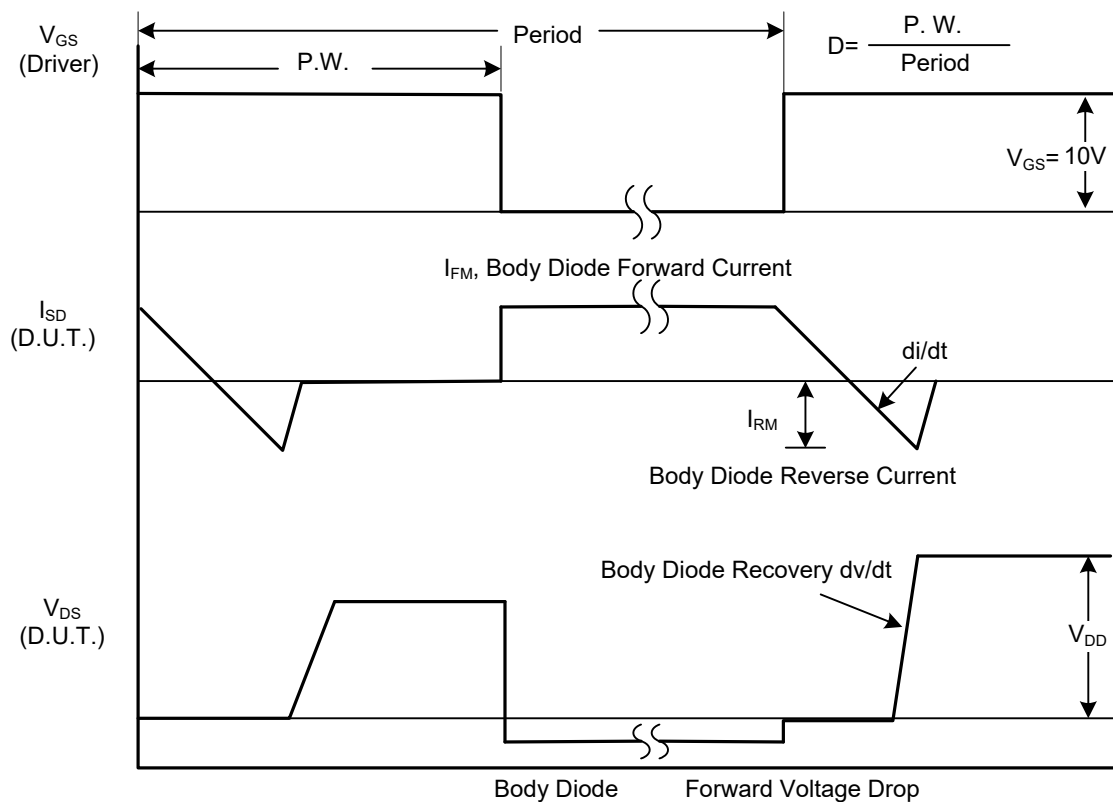
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS

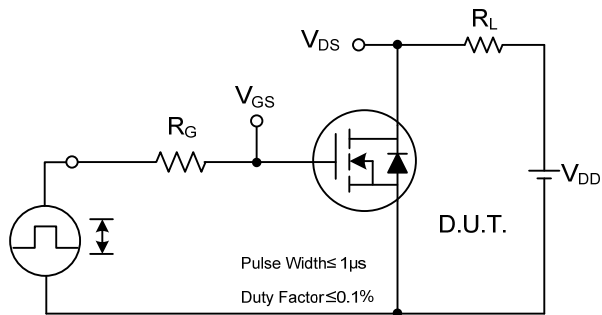


Peak Diode Recovery dv/dt Test Circuit

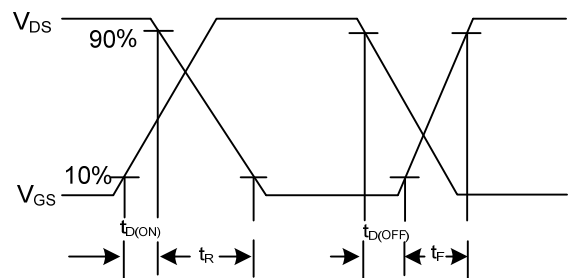


Peak Diode Recovery dv/dt Waveforms

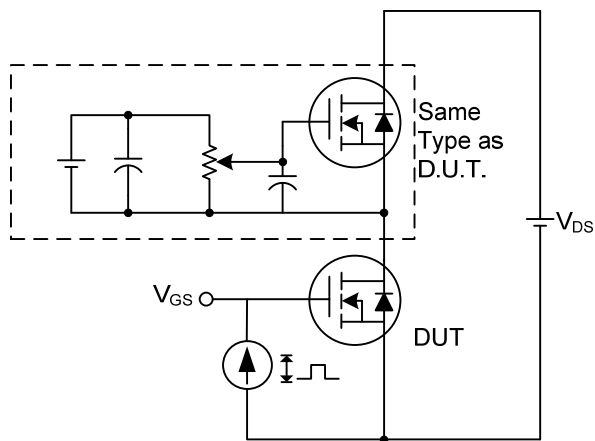
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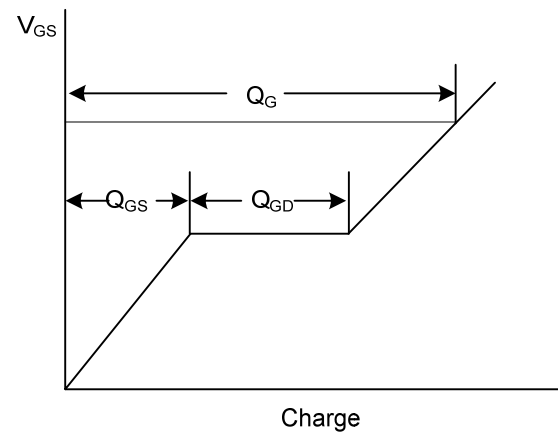
Switching Test Circuit



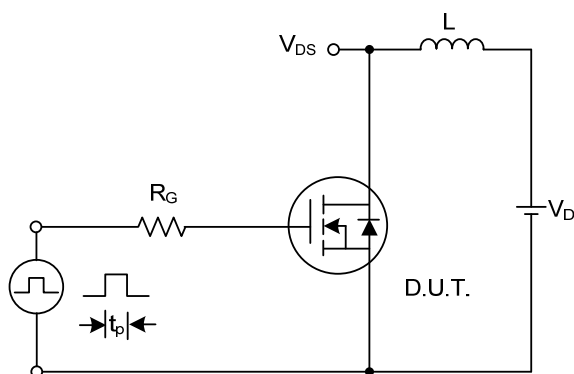
Switching Waveforms



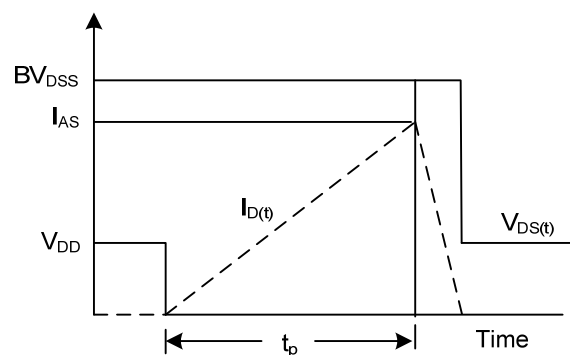
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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