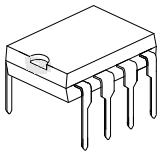
US2652SQ **Preliminary** ***CMOS IC***

LOW COST POWER-SAVING MODE PWM CONTROLLER FOR FLYBACK CONVERTERS



DIP-7A

■ DESCRIPTION

The UTC **US2652SQ** provides a CCM/valley switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, and switch to valley switching at light load.

The UTC **US2652SQ** is a high performance current mode PWM controller ideally suited for low standby power. Drain-start up cell is design to minimize the standby power to minimize the standby power. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for Higher conversion efficiency at light load condition.

The UTC **US2652SQ** contains protection with automatic recovery including OLP (over load protection), OCP (cycle-by-cycle current limiting), and UVLO (V_{DD} over voltage clamp and under voltage lockout). It also provides the protections including OTP (over temperature protection), BNO(AC Brown Out protection) , LNO(AC Over voltage protection), OVP (VCC or DC output over voltage protection) with automatic recovery. To protect the power MOSFET, Gate-drive output is fixed up to 16V max.

The internal slope compensation improves system stability at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch, which offering minima external component count in the design. Excellent EMI performance is achieved with UTC proprietary frequency hopping technique (ZL201020615247.1) together with soft driver control. Audio noise is eliminated due to switch frequency more than 20kHz during operation.

UTC **US2652SQ** has such applications as: battery charger, power adaptor, set-top box power supplies, ink jet printers, open-frame SMPS.

■ FEATURES

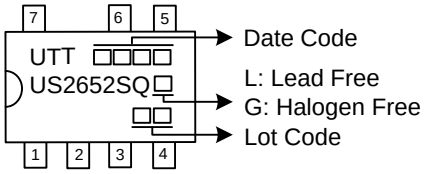
* Proprietary frequency hopping for Improved EMI performance
* Low standby power with only 30~70mw
* Cycle-by-cycle current limiting
* CCM/Valley Switching Operation
* Fixed switch frequency 65~85kHz
* Dynamic peak current limiting for constant output power
* Built-in synchronized slope compensation
* Gate output voltage clamped at 16V
* Adjustable DC output OVP
* OLP/V_{CC} OVP/OTP/BNO/LNO (automatic recovery)
* Internal Soft Start

■ ORDERING INFORMATION

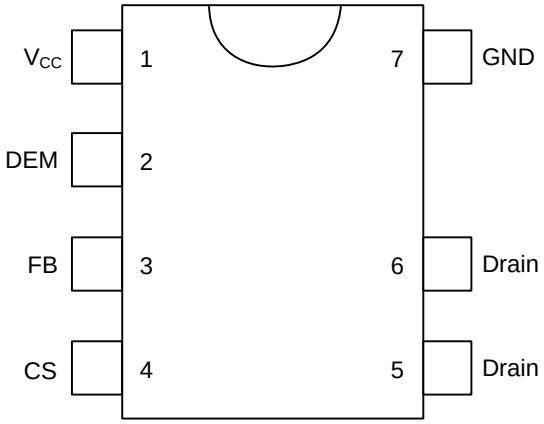
Ordering Number		Package	Packing
Lead Free	Halogen Free		
US2652SQL-D07A-T	US2652SQG-D07A-T	DIP-7A	Tube

US2652SQG-D07A-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) D07: DIP-7A (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



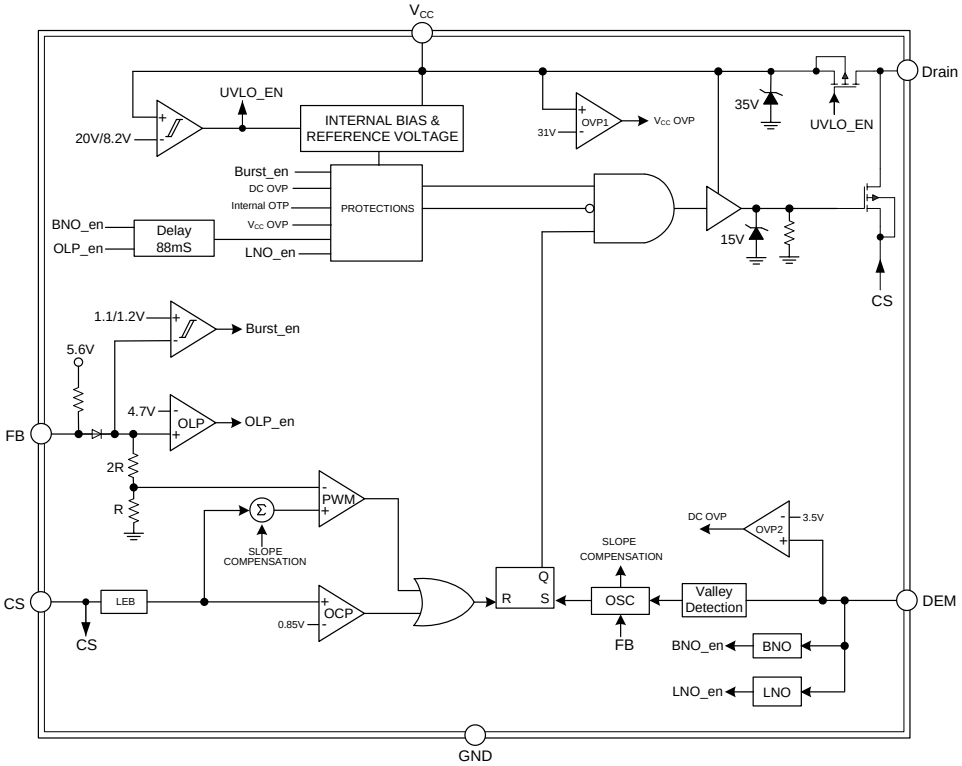
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{CC}	IC power supply pin.
2	DEM	Transformer core demagnetization detection pin. This pin is also used for output over voltage protection (Output OVP).
3	FB	Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is generated by this pin voltage and the current sense signal at Pin 4.
4	CS	Current sense input pin.
5, 6	Drain	High voltage power MOSFET drain connection.
7	GND	Ground.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.3 ~ 36	V
FB, CS, DEM		-0.3 ~ 6	V
Power Dissipation	P_D	400	mW
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	11 ~ 28	V
Start up Charge Current to CV_{CC}	I_{ch}	≥ 0.5	mA
V_{CC} Capacitor		4.7 ~ 68	μF

■ THERMAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Package Thermal Resistance	θ_{JA}	250	°C/W

■ ELECTRICAL CHARACTERISTICS (V_{CC}=15V, T_A=25°C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage						
V_{CC} (ON)			18	20	22	V
V_{CC} (OFF)			7	8.2	9.5	V
Startup Current		V_{CC}<V_{CC} (ON)-0.5V		3.5	15	μA
Operating Current		V_{FB}=3V		0.8		mA
		V_{FB}=Burst Level		0.5		mA
V_{CC} OVP Threshold			29	31	33	V
Oscillator & Switching Frequency						
Switching Frequency			60	65	70	KHz
Temperature Stability		Guaranteed by Design			10	%
Voltage Stability					10	%
Green Mode Frequency			20			KHz
Frequency Spreading Range			+9		-9	%
Max.Duty Cycle	DC_{MAX}	V_{FB}=3.9V	58	62	66	%
Voltage Feedback						
Open Loop Voltage			5.35	5.5	5.65	V
OLP Level				4.65	4.85	V
OLP De-Bounce Time		V_{FB}>5V	60	88	120	mS
Burst-Mode Enter FB Voltage	V_{FB-IN}			1.07		V
Burst-Mode Quit FB Voltage	V_{FB-OUT}			1.13		V
FB Pin Short Current				240		μA
Current Sensing						
Current Limiting Threshold Voltage with 40% Duty	$V_{CS(OFF)\_40\% Duty}$	Guaranteed by Design	0.83	0.85	0.87	V
Current Limiting Threshold Voltage with 0% Duty	$V_{CS(OFF)\_0\% Duty}$		0.52	0.57	0.62	nS
Lead Edge Blanking Time	T_{LEB}	Guaranteed by Design		350		ns
Soft Start Time				6		mS

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Drive Output						
Output Low Level		V_{CC}=15V, I_{OUT}=-20mA			1	V
Output High Level		V_{CC}=15V, I_{OUT}=20mA	9			V
Rising Time	t_R	10% to 90% of V_{OUT}, C_L=1nF		300		nS
Falling Time	t_F	90% to 10% of V_{OUT}, C_L=1nF		60		nS
Out Clamping		V_{CC}=20V		15		V
Demagnetization (DEM) Detection						
DEM OVP Sampling Instant		Guaranteed by Design		3		μS
DEM OVP Threshold Level			3.4	3.55	3.7	V
DEM OVP De-Bounce Time		Guaranteed by Design		7		Times
Demagnetization Detection Level		Guaranteed by Design		220		mV
Demagnetization Delay		Guaranteed by Design		200		nS
DEM_BNI		Guaranteed by Design	47	51	55	μA
DEM_BNO			42.5	46	49.5	μA
BNO De-Bounce Time			60	88	120	mS
Thermal Shut Down						
OTP Threshold				150		°C

■ APPLICATION NOTE

The UTC **US2652SQ** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC **US2652SQ** series.

Start-up

HV-start up cell charge to V_{CC} capacitor during V_{CC} on, and HV-start up cell is shutdwon when V_{CC} voltage is over V_{CCON} threshold. So standby power is only 30~70mw. The D1 IN4148 can improve surge capability to 6.6KV.

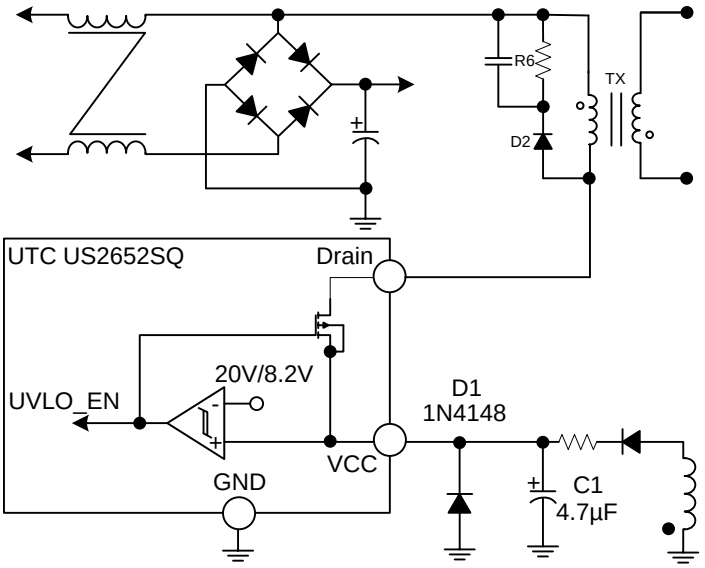
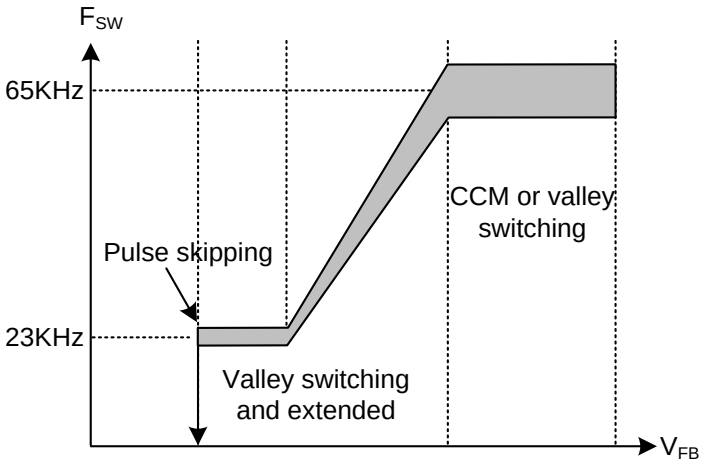


Fig. 1 Startup Circuit

Operation Mode

The UTC **US2652SQ** provides a CCM/valley switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, once if the converter enters into DCM, the UTC **US2652SQ** automatically finds the local minimum Vds point and switching at this local valley.

Normally, the conduction loss is dominated at heavy load condition, and the switching loss turns to be larger than conduction loss in light load, especially at 1/4 ~ 1/2 of full load. By this kind of mixed mode operation to have CCM in heavy load and valley switching in light load can optimize the overall average efficiency during the entire operation range.



■ APPLICATION NOTE (Cont.)

As shown in Fig. 3, at deep light-load or no-load condition, the switching loss is the dominant factor. To improve the light-load efficiency, burst mode operation will stop the switching cycle of the OUT pin when FB pin voltage is below "V_{FB_IN}" Level and restart the switching cycle of the OUT pin when FB pin voltage is above "V_{FB_OUT}".

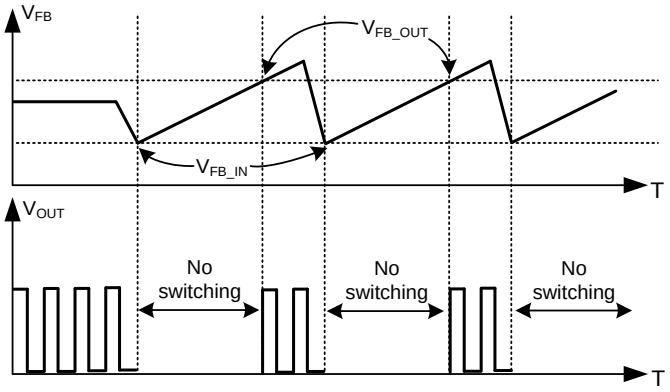


Fig. 3 Burst Mode Operation

Over Voltage Protection on V_{CC} Pin (V_{CC} OVP)

The V_{CC} OVP will shut down the switching of the power MOSFET whenever $V_{DD} > V_{OVP}$. The OVP event as followed Fig.4.

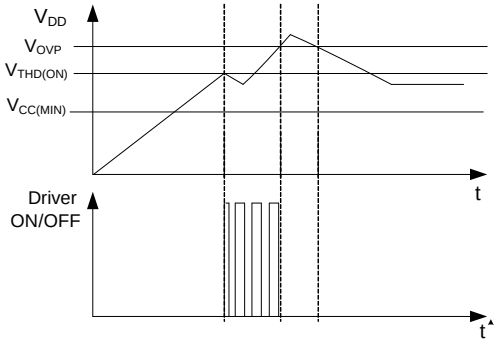


Fig.4 OVP case

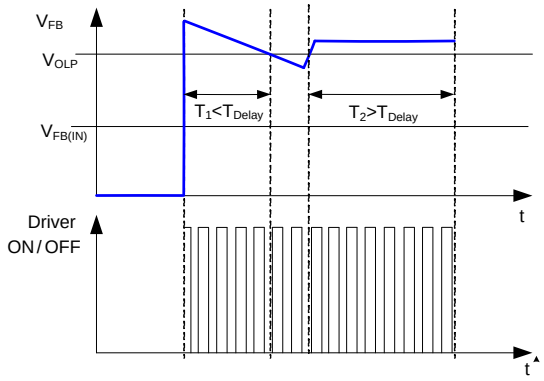


Fig.5 OLP case

Over Load &Open Loop & Output Short Protection (OLP or OSP)

OLP or OSP will shut down driver when $V_{FB} > V_{OLP}$ for continual a blanking time. The OLP or OSP event as followed Fig.5.

Over Temperature Protection (OTP)

OTP will shut down driver when the NTC resistor temperature $T_J > T_{(THR)}$.

Brown in/out & DEM OVP Protection

To prevent high current stress at too low AC voltage condition, the UTC **US2652SQ** implements an AC brown in/out protection through the DEM pin. The current sourcing out from the DEM pin when the OUT pin is enabled is monitored to have the AC input voltage level information. When the current keeps above the DEM_BNI threshold (50μA, typ.) for more than BNI De-bounce time 7 cycles, the AC brown in condition is issued and the OUT is enabled. Once if the current keeps under the DEM_BNO threshold (45.5μA, typ.) for more than BNO De-bounce time, the AC brown out condition is issued and the OUT is disabled.

■ APPLICATION NOTE (Cont.)

The equation is used to calculate the brown in/out level:

$$V_{AC\_BNI} = 50u \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}} \quad , \quad V_{AC\_BNO} = 45.5u \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}}$$

An over voltage protection for Vo is fulfilled by sampling the voltage on the DEM waveform after OUT is turn-off. After a short delay after OUT off, the sampled voltage is compared to the internal over voltage reference is determined whether if an OVP event is occurred. The internal over voltage reference is biased at 3.5V, uses can define the resistor divider ratio by the equation below based on the desired OVP level:

$$V_{O\_OVP} = 3.5 \times \frac{R_{DEM\_U} + R_{DEM\_D}}{R_{DEM\_D}} \times \frac{N_{SEC}}{N_{AUX}}$$

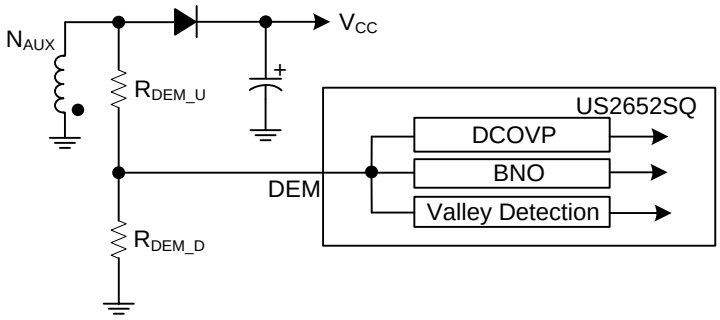


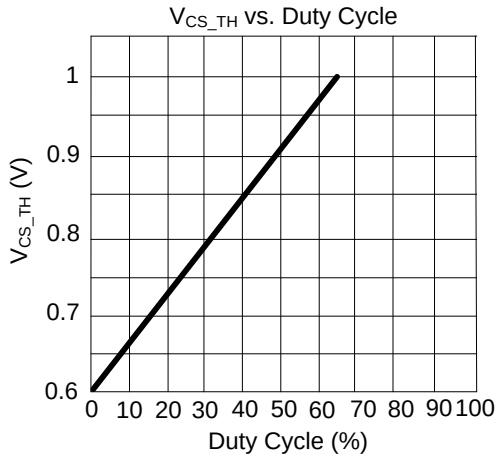
Fig. 6 DEM-Pin Divider

Cycle by Cycle Over-Current Protection (OCP)

In a Flyback topology converter, the main MOSFET switch of the Flyback converter turns on and off rapidly. The energy is stored in the inductor when the MOSFET turns on. The inductor current flowing through the sensing resistor (R_{CS}) is shown in Fig.7. The current limit is determined by the equation below:

$$I_{PEAK} = \frac{V_{CS}}{R_{CS}}$$

In order to prevent the CS pin from false triggering, an internal leading edge blanking time (350nS Typ.) is added.



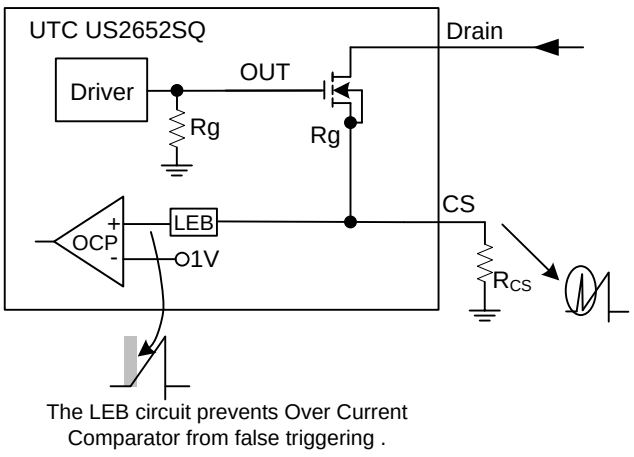
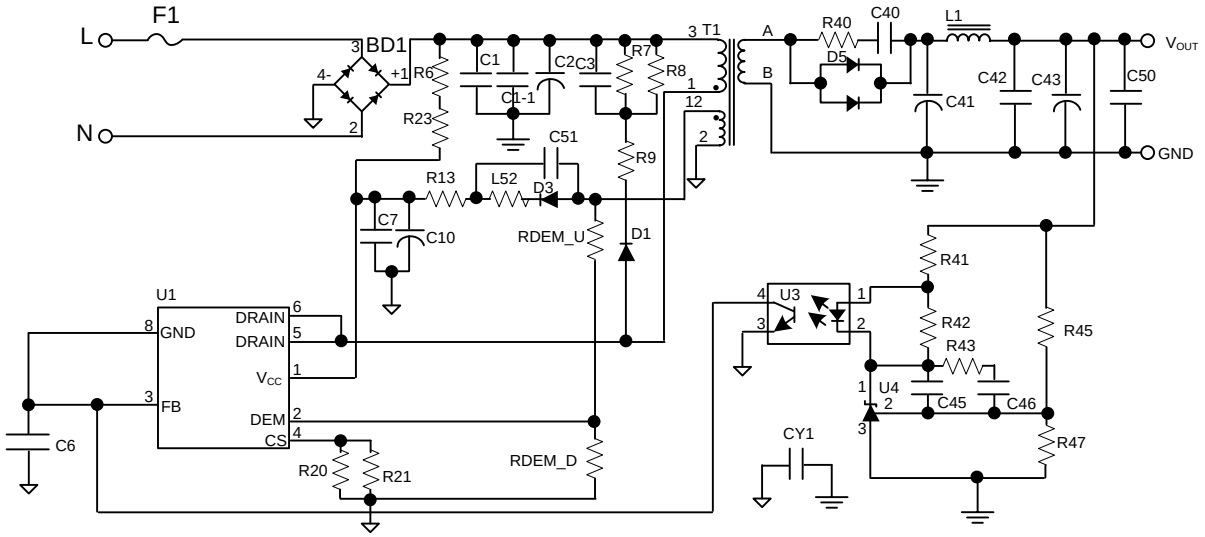


Fig. 7 Current Sensing

■ TYPICAL APPLICATION CIRCUIT



BOM

Reference	Component	Reference	Component
BD1	2A_600V	C1,C3	C 1nF/1KV
C2	ELC 22μF/400V, 105 C, ±20%	C10	ELC 10μF/50V, 105 C, ±20%
C7	C 0.1uF/50V	C6	C 1nF/50V
C41,C43	ELC 680μF/16V, 105 C, ±20%	C46	C 0.1uF/50V
C45	C 10nF/50V	C40	C 1nF/1KV
F1	Fuse 1A/250V	T1	RM8 66:9:10 Lp=2.60mH
L1	R Core φ0.8 1uH	L52	R 0Ω
R9	R 0Ω	R7,R8	R 1MΩ
R13	R 1Ω	R20	R 3.6Ω
R21	R 3.9Ω	R40	R 1KΩ
R46	R 10KΩ	R45	R 39KΩ
R42	R 2.2KΩ	R41	R 510Ω
RDEM_U	R 360KΩ	R43	R 680Ω
CY1	Y-Cap 1000pF/400V	RDEM_D	R 200KΩ//180KΩ
D3	BAV20W 1A/200V	U3	LTV-357-T-C
D4	1N4148 0.15A/75V	D1	1N4007 1A/1000V
D5	MGBR30V100CL 30A/100V	U4	TL431
U1	UTC US2652SQ	No Component	R6,R23,C51,C42,C50,C1-1