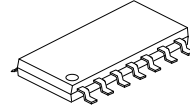


**UCD4071B****CMOS IC****QUAD 2-INPUT OR
BUFFERED B SERIES GATE****■ DESCRIPTION**

The **UTC UCD4071B** contains four independent 2-input OR gates and they perform the function $Y=A+B$ in positive logic.

■ FEATURES

- * 5V-10V-15V Parametric Ratings
- * Quad 2-Input OR Gate
- * Symmetrical Output Characteristics
- * Maximum Input Current of 1uA at 15V Over Full Package Temperature
- * Low Power TTL:
Fan Out of 2 Driving 74L or 1 Driving 74LS Compatibility

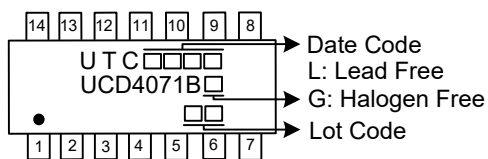


SOP-14U

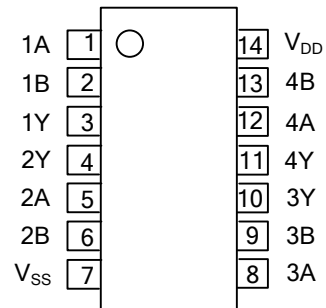
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4071BL-UEA-R	UCD4071BG-UEA-R	SOP-14U	Tape Reel

UCD4071BG-UEA-R	(1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) UEA: SOP-14U (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING

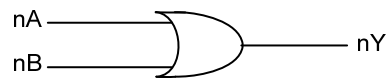
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	H
H	L	H
L	H	H
L	L	L

■ LOGIC DIAGRAM (positive logic)



■ **ABSOLUTE MAXIMUM RATING** (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{DD}	-0.5 ~ 18	V
Input Voltage	V(nA,nB)	-0.5 ~ V _{DD} +0.5	V
Output Voltage	V(nY)	-0.5 ~ V _{DD} +0.5	V
Storage Temperature	T _{STG}	-65 ~ + 150	°C
Lead Temperature(Soldering,10s)	T _L	+260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{DD}	3 ~ 15	V
Operating Temperature	T _{OP}	-40 ~ +125	°C

■ **ELECTRICAL CHARACTERISTICS** (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V _{IH}	V _{DD} = 5V, V _O =0.5V	3.5	3		V
		V _{DD} = 10V, V _O =1.0V	7.0	6		V
		V _{DD} = 15V, V _O =1.5V	11.0	9		V
Low-Level Input Voltage	V _{IL}	V _{DD} = 5V, V _O =4.5V		2	1.5	V
		V _{DD} = 10V, V _O =9.0V		4	3.0	V
		V _{DD} = 15V, V _O =13.5V		6	4.0	V
High-Level Output Voltage	V _{OH}	V _{DD} = 5V, I _{OH} =1μA	4.95	5		V
		V _{DD} = 10V, I _{OH} =1μA	9.95	10		V
		V _{DD} = 15V, I _{OH} =1μA	14.95	15		V
Low-Level Output Voltage	V _{OL}	V _{DD} = 5V, I _{OL} =1μA		0	0.05	V
		V _{DD} = 10V, I _{OL} =1μA		0	0.05	V
		V _{DD} = 15V, I _{OL} =1μA		0	0.05	V
High-Level Output Current (NOTE)	I _{OH}	V _{DD} = 5V, V _O =4.6V	-0.51	-0.88		mA
		V _{DD} = 10V, V _O =9.5V	-1.3	-2.25		mA
		V _{DD} = 15V, V _O =13.5V	-3.4	-8.8		mA
Low-Level Output Current (NOTE)	I _{OL}	V _{DD} = 5V, V _O =0.4V	0.51	0.88		mA
		V _{DD} = 10V, V _O =0.5V	1.3	2.25		mA
		V _{DD} = 15V, V _O =1.5V	3.4	8.8		mA
Input Leakage Current	I _{I(LEAK)}	V _{DD} = 15V, V _{IN} = V _{DD} or GND			0.1	μA
Quiescent Supply Current	I _Q	V _{DD} = 5V, V _{IN} = V _{DD} or V _{SS} , I _{OUT} = 0		0.004	0.25	μA
		V _{DD} = 10V, V _{IN} = V _{DD} or V _{SS} , I _{OUT} = 0		0.005	0.5	μA
		V _{DD} = 15V, V _{IN} = V _{DD} or V _{SS} , I _{OUT} = 0		0.006	1.0	μA

Note: I_{OL} and I_{OH} are tested one output at a time

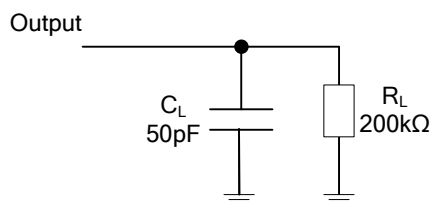
■ **SWITCHING CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$, Input: $t_R=t_F=20\text{ns}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	t_{PLH}	$V_{DD}=5\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		90	250	ns
		$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	100	ns
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		30	70	ns
	t_{PHL}	$V_{DD}=5\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		100	250	ns
		$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	100	ns
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		30	70	ns
Transition Time	t_{TLH}	$V_{DD}=5\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		90	200	ns
	t_{THL}	$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		50	100	ns
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	80	ns

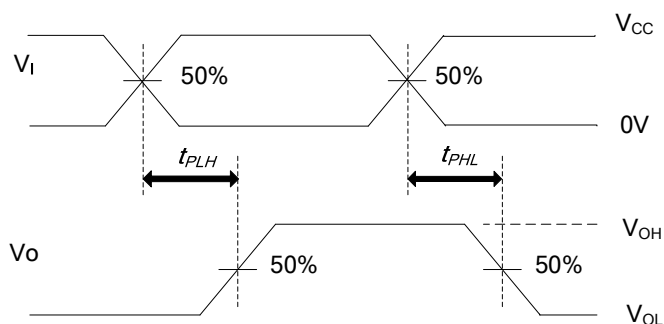
■ **OPERATING CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		5	7.5	pF
Power Dissipation Capacitance	C_{PD}	Any Gate		18		pF

■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit



Propagation Delay Times

Note: C_L includes probe and jig capacitance.

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