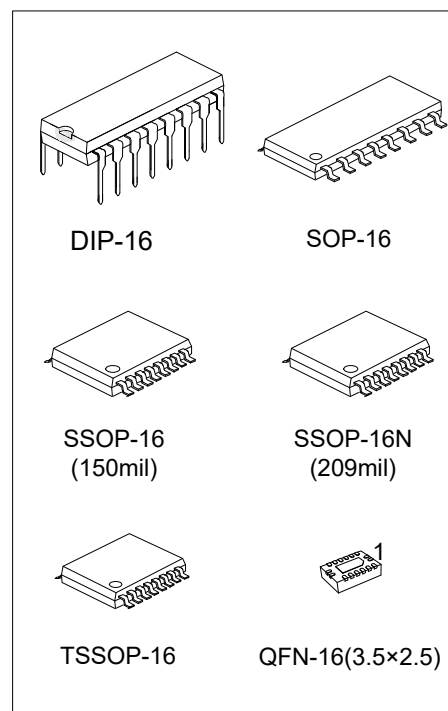


**U74HC595B****CMOS IC****8-BIT SERIAL-IN SHIFT
REGISTER WITH LATCHED
3-STATE PARALLEL OUTPUTS,
PROVIDING SERIAL OUTPUT****■ DESCRIPTION**

The UTC **U74HC595B** contains an 8-bit register with asynchronous reset input and an 8-bit latch with output. The Serial Data Input (SER) will shift into the internal shift register during every LOW-to-HIGH transition on the Shift Clock. The latch will latch the 8-bit data from the shift register during the LOW-to-HIGH transition on the Latch Clock. The shift register also provides a serial output.

■ FEATURES

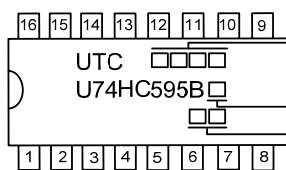
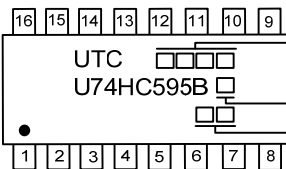
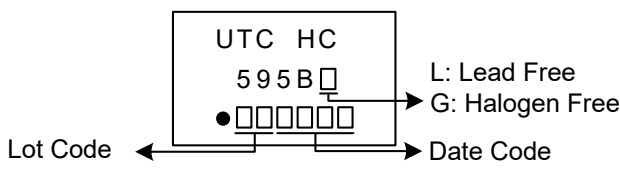
- * Operation Voltage Range: 2 ~ 6V
- * High Noise Immunity
- * Output Compatibility with CMOS and TTL
- * Specified from -40 ~ +125°C

**■ ORDERING INFORMATION**

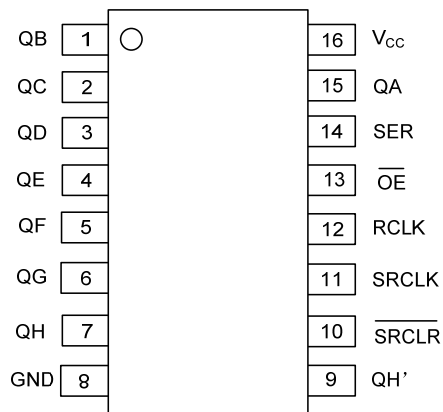
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC595BL-D16-T	U74HC595BG-D16-T	DIP-16	Tube
U74HC595BL-S16-R	U74HC595BG-S16-R	SOP-16	Tape Reel
U74HC595BL-R16-R	U74HC595BG-R16-R	SSOP-16	Tape Reel
U74HC595BL-R16N-R	U74HC595BG-R16N-R	SSOP-16N	Tape Reel
U74HC595BL-P16-R	U74HC595BG-P16-R	TSSOP-16	Tape Reel
U74HC595BL-QAH-R	U74HC595BG-QAH-R	QFN-16(3.5×2.5)	Tape Reel

U74HC595BG-D16-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) D16: DIP-16, S16: SOP-16, R16: SSOP-16, R16N: SSOP-16N, P16: TSSOP-16 QAH: QFN-16(3.5×2.5) (3) G: Halogen Free and Lead Free, L: Lead Free
--	---

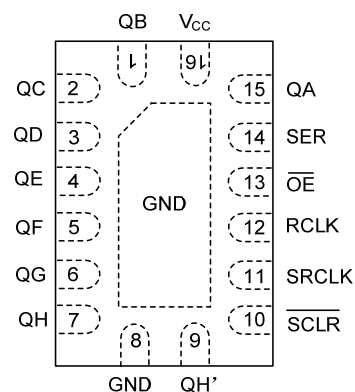
MARKING

PACKAGE	MARKING
DIP-16	 UTC □ □ □ □ → Date Code U74HC595B □ → L: Lead Free □ → G: Halogen Free □ □ □ → Lot Code
SOP-16 / SSOP-16 SSOP-16N / TSSOP-16	 UTC □ □ □ □ → Date Code U74HC595B □ → L: Lead Free □ → G: Halogen Free □ □ □ → Lot Code
QFN-16(3.5×2.5)	 UTC HC 595B □ → L: Lead Free □ □ □ → G: Halogen Free □ □ □ → Lot Code □ □ □ □ → Date Code

PIN CONFIGURATION



DIP-16 / SOP-16 / SSOP-16
SSOP-16N / TSSOP-16



QFN-16(3.5×2.5)
(TOP VIEW)

FUNCTION TABLE

FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	QH'	Qn
A Low-Level on $\overline{SRCLR}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑	L	H	X	QG'	Qn'

Note: H : HIGH voltage level.

L : LOW voltage level.

X : Don't care.

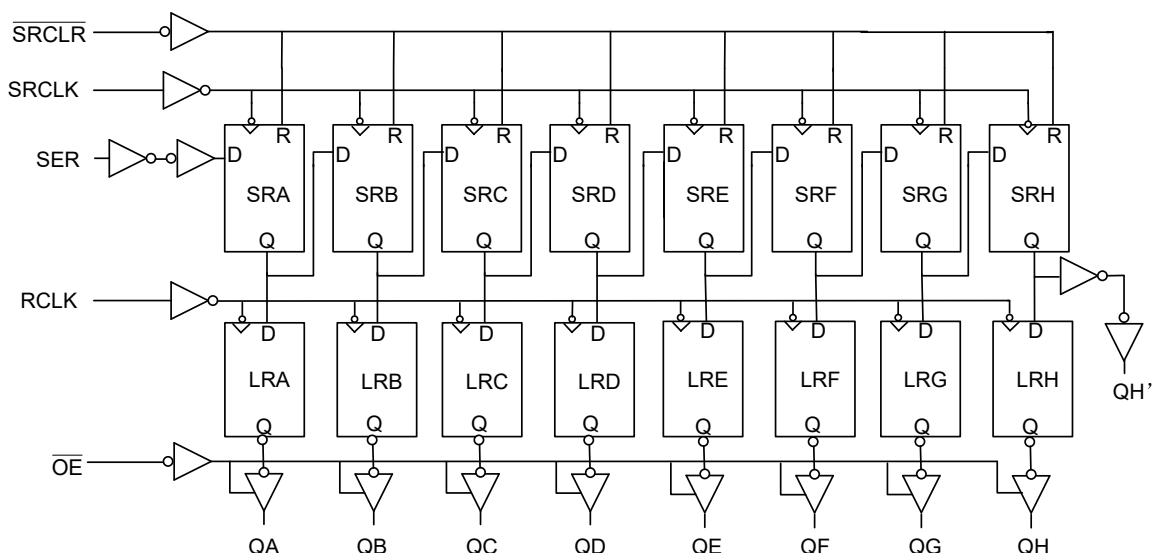
Z : High impedance OFF-state.

NC: No change.

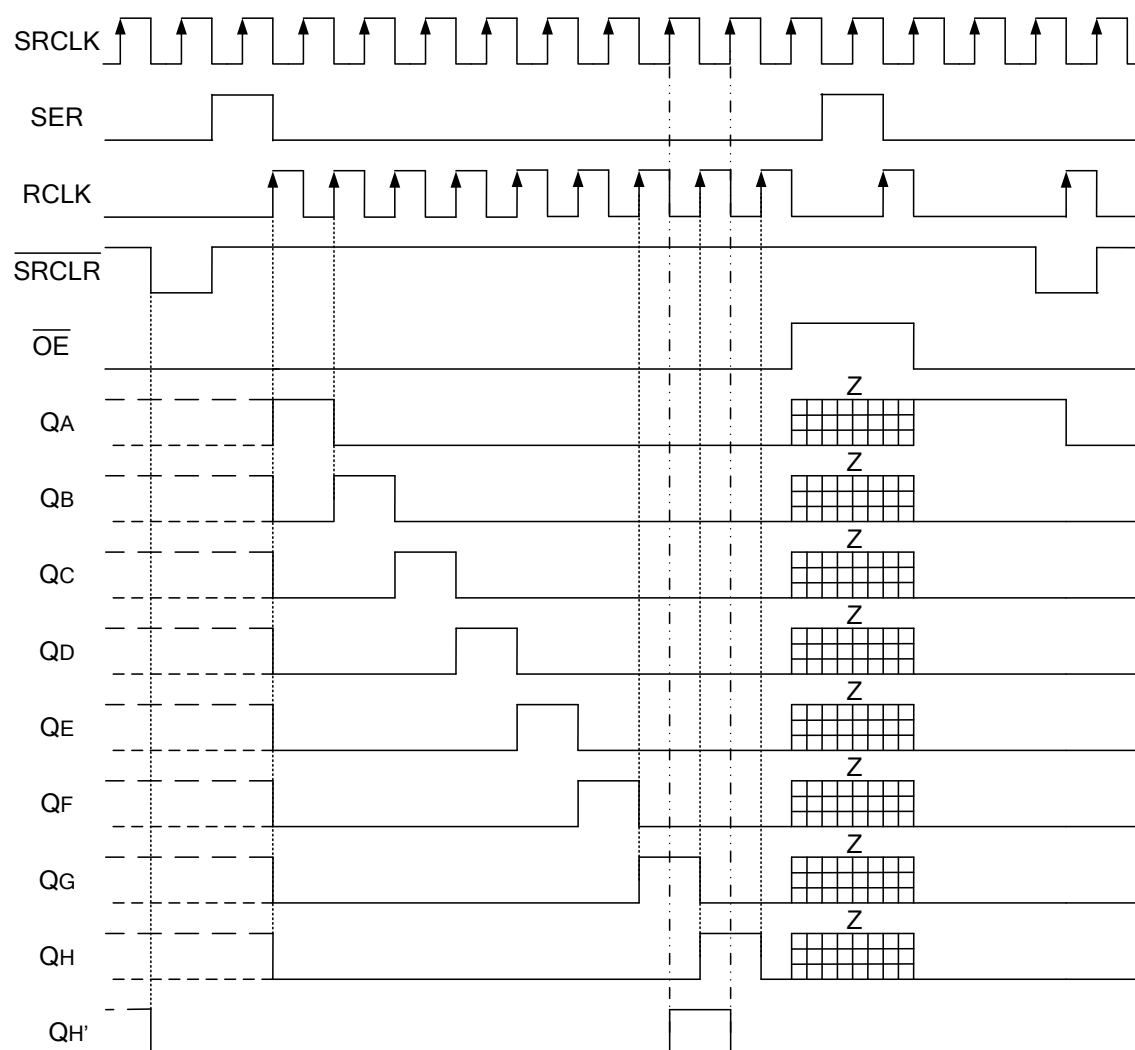
↑ : Low-to-High transition.

↓ : High-to-Low transition.

LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Note 1)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5~7.0	V
Input Clamp Current ($V_{IN} < 0$ or $V_{IN} > V_{CC}$)		I_{IK} (Note 2)	± 20	mA
Output Clamp Current ($V_{OUT} < 0$ or $V_{OUT} > V_{CC}$)		I_{OK} (Note 2)	± 20	mA
Output Current		I_{OUT}	± 35	mA
V_{CC} or GND Current		I_{CC}	± 75	mA
Power Dissipation	DIP-16	P_D	750	mW
	SOP-16		500	mW
	SSOP-16		450	mW
	SSOP-16N			
	TSSOP-16		400	mW
	QFN-16(3.5×2.5)			
Storage Temperature		T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	2		6	V
Input Voltage		V_{IN}	0		V_{CC}	V
Output Voltage		V_{OUT}	0		V_{CC}	V
Operating Temperature		T_A	-40		+125	°C
Input Transition Rise or Fall Time	$V_{CC}=2V$	t_R / t_F			200	ns
	$V_{CC}=4.5V$				100	ns
	$V_{CC}=6V$				100	ns

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V _{IH}	V _{CC} =2V	1.5			1.5			V
		V _{CC} =3V	2.1			2.1			V
		V _{CC} =4.5V	3.15			3.15			V
		V _{CC} =6V	4.2			4.2			V
Low-Level Input Voltage	V _{IL}	V _{CC} =2V			0.5			0.5	V
		V _{CC} =3V			0.9			0.9	V
		V _{CC} =4.5V			1.35			1.35	V
		V _{CC} =6V			1.8			1.8	V
High-Level Output Voltage, Q _A -Q _H	V _{OH}	V _{CC} =2V, I _{OH} =-20μA	1.9	2.0		1.9			V
		V _{CC} =4.5V, I _{OH} =-20μA	4.4	4.5		4.4			V
		V _{CC} =6V, I _{OH} =-20μA	5.9	6.0		5.9			V
		V _{CC} =3V, I _{OH} =-2.4mA	2.48			2.3			V
		V _{CC} =4.5V, I _{OH} =-6mA	3.98			3.7			V
		V _{CC} =6V, I _{OH} =-7.8mA	5.48			5.2			V
Low-Level Output Voltage, Q _A -Q _H	V _{OL}	V _{CC} =2V, I _{OL} =20μA		0.002	0.1			0.1	V
		V _{CC} =4.5V, I _{OL} =20μA		0.001	0.1			0.1	V
		V _{CC} =6V, I _{OL} =20μA		0.001	0.1			0.1	V
		V _{CC} =3V, I _{OL} =2.4mA			0.26			0.4	V
		V _{CC} =4.5V, I _{OL} =6mA			0.26			0.4	V
		V _{CC} =6V, I _{OL} =7.8mA			0.26			0.4	V
High-Level Output Voltage, Q _H '	V _{OH}	V _{CC} =2V, I _{OH} =-20μA	1.9	2.0		1.9			V
		V _{CC} =4.5V, I _{OH} =-20μA	4.4	4.5		4.4			V
		V _{CC} =6V, I _{OH} =-20μA	5.9	6.0		5.9			V
		V _{CC} =3V, I _{OH} =-2.4mA	2.48			2.3			V
		V _{CC} =4.5V, I _{OH} =-4mA	3.98			3.7			V
		V _{CC} =6V, I _{OH} =-5.2mA	5.48			5.2			V
Low-Level Output Voltage, Q _H '	V _{OL}	V _{CC} =2V, I _{OL} =20μA		0.002	0.1			0.1	V
		V _{CC} =4.5V, I _{OL} =20μA		0.001	0.1			0.1	V
		V _{CC} =6V, I _{OL} =20μA		0.001	0.1			0.1	V
		V _{CC} =3V, I _{OL} =2.4mA			0.26			0.4	V
		V _{CC} =4.5V, I _{OL} =4mA			0.26			0.4	V
		V _{CC} =6V, I _{OL} =5.2mA			0.26			0.4	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =6V, V _{IN} =V _{CC} or GND			±0.1			±1	μA
Output Off-State Current	I _{OZ}	V _{CC} =6V, V _{OUT} =V _{CC} or GND			±0.5			±10	μA
Quiescent Supply Current	I _{CC}	V _{CC} =6V, V _{IN} =V _{CC} or GND, I _{OUT} =0			4			160	μA

■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		T _A =25°C			T _A =-40°C~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Clock Pulse Frequency	f _{max}	V _{CC} =2V	C _L =50pF	5	9		3			MHz
		V _{CC} =4.5V		15	28		9			MHz
		V _{CC} =6V		18	32		12			MHz
Propagation Delay From Input (SRCLK) to Output (Q _{H'})	t _{PD}	V _{CC} =2V	C _L =50pF		105	160			285	ns
		V _{CC} =4.5V			35	60			100	ns
		V _{CC} =6V			31	50			80	ns
Propagation Delay From Input (RCLK) to Output (Q _A -Q _H)		V _{CC} =2V	C _L =50pF		25	140			265	ns
		V _{CC} =4.5V			17	28			53	ns
		V _{CC} =6V			14	24			45	ns
		V _{CC} =2V	C _L =150pF		25	200			250	ns
		V _{CC} =4.5V			17	40			50	ns
		V _{CC} =6V			14	34			43	ns
Propagation Delay From Input (SRCLR) to Output (Q _{H'})	t _{PHL}	V _{CC} =2V	C _L =50pF		86	145			265	ns
		V _{CC} =4.5V			30	50			90	ns
		V _{CC} =6V			26	45			80	ns
Propagation Delay From Input ($\overline{\text{OE}}$) to Output (Q _A -Q _H)	t _{en}	V _{CC} =2V	C _L =50pF		25	135			225	ns
		V _{CC} =4.5V			15	27			45	ns
		V _{CC} =6V			10	23			38	ns
		V _{CC} =2V	C _L =150pF		50	200			250	ns
		V _{CC} =4.5V			23	40			50	ns
		V _{CC} =6V			19	34			43	ns
Propagation Delay From Input ($\overline{\text{OE}}$) to Output (Q _A -Q _H)	t _{dis}	V _{CC} =2V	C _L =50pF		25	150			250	ns
		V _{CC} =4.5V			15	30			50	ns
		V _{CC} =6V			10	26			43	ns
Output Transition Time (Q _A -Q _H)	t _t	V _{CC} =2V	C _L =50pF		25	60			75	ns
		V _{CC} =4.5V			8	12			15	ns
		V _{CC} =6V			6	10			13	ns
		V _{CC} =2V	C _L =150pF		25	210			265	ns
		V _{CC} =4.5V			15	42			53	ns
		V _{CC} =6V			10	36			45	ns
Output Transition Time (Q _{H'})		V _{CC} =2V	C _L =50pF		25	75			95	ns
		V _{CC} =4.5V			8	15			19	ns
		V _{CC} =6V			6	13			16	ns

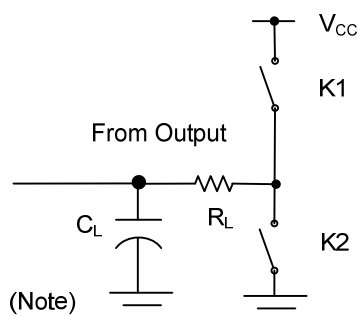
■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Pulse Duration, SRCLK or RCLK High or Low	t _w	V _{CC} =2V	80			110			ns
		V _{CC} =4.5V	16			22			ns
		V _{CC} =6V	14			19			ns
V _{CC} =2V		80			110			ns	
V _{CC} =4.5V		16			22			ns	
V _{CC} =6V		14			19			ns	
Setup Time, SER Before SRCLK↑	t _{su}	V _{CC} =2V	100			125			ns
		V _{CC} =4.5V	20			25			ns
		V _{CC} =6V	17			21			ns
V _{CC} =2V		75			94			ns	
V _{CC} =4.5V		15			19			ns	
V _{CC} =6V		13			16			ns	
Setup Time, $\overline{\text{SRCLR}}$ Low Before RCLK↑		V _{CC} =2V	50			65			ns
		V _{CC} =4.5V	10			13			ns
		V _{CC} =6V	9			11			ns
Setup Time, $\overline{\text{SRCLR}}$ High (inactive) Before SRCLK↑		V _{CC} =2V	50			60			ns
		V _{CC} =4.5V	10			12			ns
		V _{CC} =6V	9			11			ns
Hold Time, SER After SRCLK↑	t _H	V _{CC} =2V	3			3			ns
		V _{CC} =4.5V	3			3			ns
		V _{CC} =6V	3			3			ns

■ OPERATING CHARACTERISTIC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C _{IN}	V _{CC} =6V, V _{IN} =V _{CC} or GND			10	pF
Power Dissipation Capacitance	C _{PD}	No load		400		pF

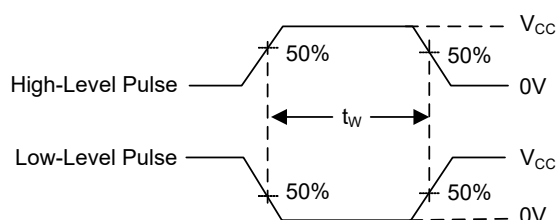
TEST CIRCUIT AND WAVEFORMS



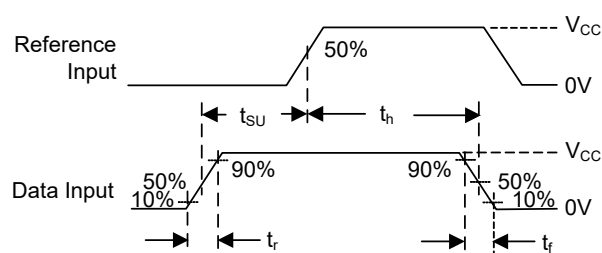
TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

t_{PD} is the same as t_{PHL} and t_{PLH} .
 t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{dis} is the same as t_{PLZ} and t_{PHZ} .

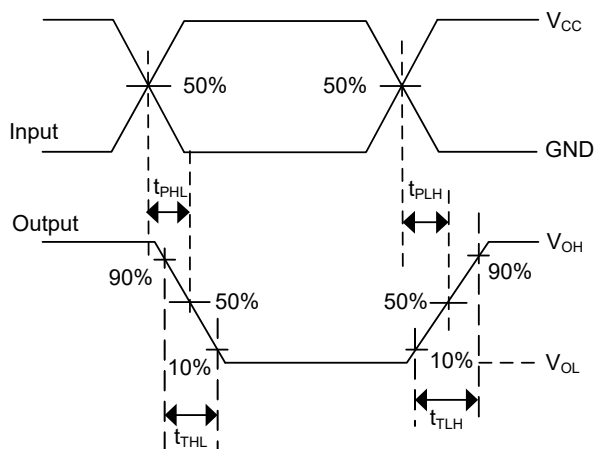
Note: C_L includes probe and jig capacitance. $C_L=50\text{pF}$ or 150pF , $R_L=1\text{K}\Omega$



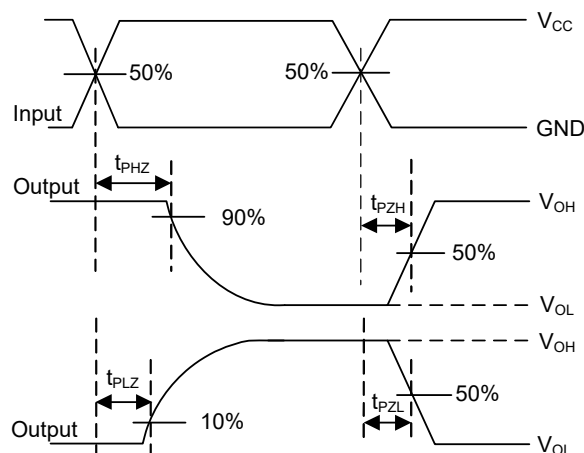
Voltage Waveforms, Pulse Duration



Voltage Waveforms



Voltage Waveforms Propagation Delays



Voltage Waveforms Propagation Delays

Note: All input pulses are supplied by generators having the following characteristics:

$P_{RR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.