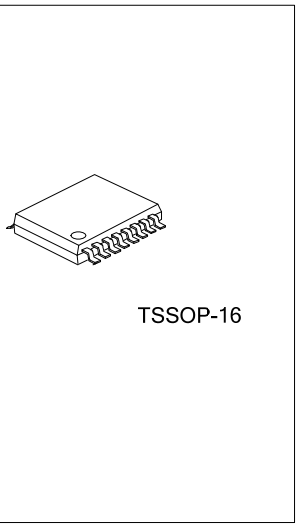
4-BIT 1 OF 2 FET MULTIPLEXER/DEMULTIPLEXER 2.5V-/3.3V LOW-VOLTAGE HIGH BANDWIDTH BUS SWITCH



■ DESCRIPTION

The **U74CB3Q3257** device is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (R_{ON}).

■ EATURES

* High-Bandwidth Data Path(up to 500MHz)
* 5V Tolerant I/Os With Device Powered Up or Powered Down
* Low and Flat ON-State Resistance (R_{ON}) Characteristics Over Operating Range (R_{ON} =4Ω Typ.)
* Rail-to-Rail Switching on Data I/O Ports
  - 0-to 5-V Switching With 3.3-V V_{CC}
  - 0-to 3.3-V Switching With 2.5-V V_{CC}
* Bidirectional Data Flow With Near-Zero Propagation Delay
* Low Input / Output Capacitance Minimizes Loading and Signal Distortion
* Fast Switching Frequency (f_{OE}=20MHz Max)
* Data and Control Inputs Provide Undershoot Clamp Diodes
* Low Power Consumption (ICC=1mA Typical)
* V_{CC} Operating Range From 2.3V to 3.6V
* Data I/Os Support 0 to 5V Signaling Levels (0.8V,1.2V,1.5V,1.8V,2.5V,3.3V,5V)
* Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
* Ioff Supports Partial-Power-Down Mode Operation
* Latch-Up Performance Exceeds100mA Per JESD 78, Class II
* Supports Both Digital and Analog Applications :PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

■ ORDERING INFORMATION

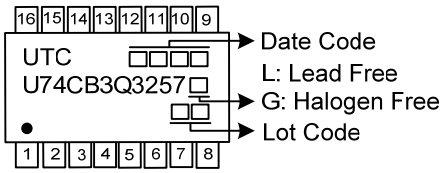
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CB3Q3257L-P16-R	U74CB3Q3257G-P16-R	TSSOP-16	Tape Reel

U74CB3Q3257G-P16-R

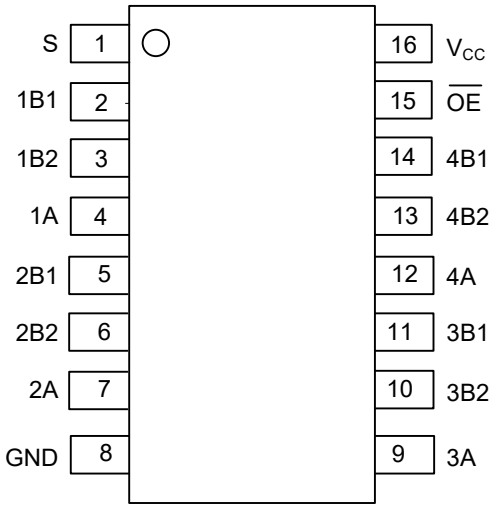
(1)Packing Type
(2) Package Type
(3) Green Package

(1) R: Tape Reel
(2) P16: TSSOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



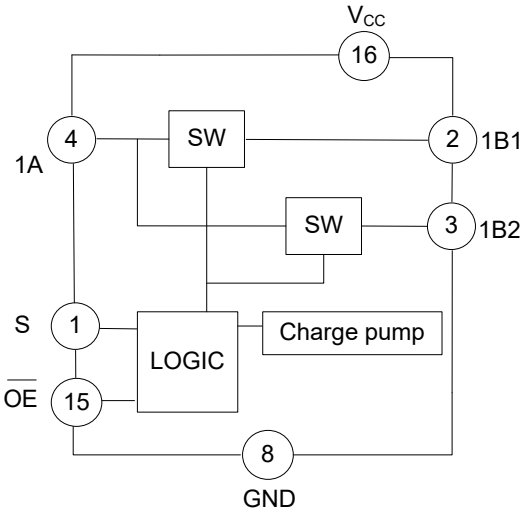
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	S	I	Select PIN
4,7,9,12	An	I/O	Input/output An.
8	GND		Ground
2,3,5,6,10, 11,13,14	Bn	I/O	Input/output Bn
15	OE	I	Output enable (Active Low)
16	V_{CC}		supply voltage

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 4.6	V
Input Voltage	V_{IN}		-0.5 ~ 7	V
Switch I/O voltage range	$V_{I/O}$		-0.5 ~ 7	V
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
I/O Port Clamp Current	$I_{I/OK}$	$V_{I/O}$<0V	-50	mA
On state switch current	I_{IO}		±64	mA
Continuous current through V_{CC} or GND			±100	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
Input / Output Voltage	$V_{I/O}$		0		5.5	V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP (Note 2)	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=2.3V~2.7V		1.7		5.5	V
		V_{CC}=2.7V~3.6V		2		5.5	V
Low-Level Input Voltage	V_{IL}	V_{CC}=2.3V~2.7V		0		0.7	V
		V_{CC}=2.7V~3.6V		0		0.8	V
Input Clamping Voltage	V_{IK}	V_{CC}=3.6V, I_I= -18mA				-1.8	V
Input Leakage Current	I_{IN}	V_{CC}=3.6V, V_{IN} = 0~5.5V		-1		1	μA
Power OFF Leakage Current	I_{OFF}	V_O=0~5.5V, V_{CC}=0V, V_I=0V				1	μA
Output OFF-State Current	I_{OZ}	V_{CC}=3.6V, V_O=0V~5.5V, V_I=0, V_{IN}=V_{CC} or GND, Switch Off		-1		1	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND, $I_{I/O}$=0A, V_{CC}=3.6V, Switch ON or OFF			1	2	mA
Additional Supply Current	ΔI_{CC}	V_{CC}=3.6V, one input at 3V,other inputs at V_{CC} or GND				30	μA
Input Capacitance	C_{IN}	V_{CC}=3.3V, V_{IN}=5.5V, 3.3V, 0			2.5	3.5	pF
OFF-State Capacitance	$C_{IO(OFF)}$	V_{CCA}=3.3V, V_{IN}=5.5V, 3.3V, 0 V_{IN}=V_{CC} or GND, Switch OFF			3.5	5	pF
ON-State Capacitance	$C_{IO(ON)}$	V_{CCA}=3.3V, V_{IN}=5.5V, 3.3V, 0 V_{IN}=V_{CC} or GND, Switch ON			9	11	pF
ON Resistane	R_{ON}	V_{CC}=2.3V	V_I=0, I_O=30mA		4	8	Ω
			V_I=1.7, I_O=-15mA		4	9	Ω
		V_{CC}=3V	V_I=0, I_O=30mA		4	6	Ω
			V_I=2.4, I_O=-15mA		4	8	Ω

Notes: 1. V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
2. All typical values are at V_{CC}=3.3V (unless otherwise noted), T_A=25°C.

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input ($\overline{OE}$ or S) to output (A or B)	$F_{\overline{OE}}$, F_S	V_{CC}=2.3V~2.7V			10	MHz
		V_{CC}=3V~3.6V			20	MHz
From input (S) to output (B or A)	t_{pd} (t_{PLH}/t_{PHL})	V_{CC}=2.3V~2.7V	1.5		10.9	ns
		V_{CC}=3V~3.6V	1.5		7.8	ns
From input ($\overline{OE}$) to output (A or B)	t_{en} (t_{PZL}/t_{PZH})	V_{CC}=2.3V~2.7V	1.5		9.9	ns
		V_{CC}=3V~3.6V	1.5		7.8	ns
From input (S) to output (B or A)		V_{CC}=2.3V~2.7V	1.5		10.5	ns
		V_{CC}=3V~3.6V	1.5		8.1	ns
From input ($\overline{OE}$) to output (A or B)	t_{dis} (t_{PLZ}/t_{PHZ})	V_{CC}=2.3V~2.7V	1		10.1	ns
		V_{CC}=3V~3.6V	1		7.5	ns
From input (S) to output (B or A)		V_{CC}=2.3V~2.7V	1		11.1	ns
		V_{CC}=3V~3.6V	1		7.8	ns

■ DETAILED DESCRIPTION

Overview

The UTC **U74CB3Q3257** device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (ron). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, The UTC **U74CB3Q3257** device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The UTC **U74CB3Q3257** device is organized as two1-of-4 multiplexers/ demultiplexers with separate output-enable(1OE,2OE)inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When OE is low, the associated multiplexer/ demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current back flow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pull up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURE DESCRIPTION

The UTC **U74CB3Q3257** device has a high-bandwidth data path(up to 500MHz) and has 5Vtolerant I/Os with the device powered up or powered down. It also has low and flat ON-state resistance (R_{ON}) characteristics over operating range (R_{ON} =4Ω Typ.).

This device also has rail-to-rail switching on data I/O ports for 0 to 5V switching with 3.3V V_{CC} and 0 to 3.3V switching with 2.5V V_{CC} as well as bidirectional data flow with near-zero propagation delay and low input/output capacitance that minimizes loading and signal distortion ($C_{IO(OFF)}$=3.5pF Typ.).

The UTC **U74CB3Q3257** also provides a fast switching frequency (f_{OE}=20MHz Max.)with data and control inputs that provide undershoot clamp diodes as well as low power consumption (I_{CC}=0.6mA Typ.).

The V_{CC} operating range is from 2.3V to 3.6V and the data I/Os support 0 to 5V signal levels of (0.8V, 0.2V,1.5V, 1.8V, 2.5V, 3.3V, 5V).

The control inputs can be driven by TTL or 5V/3.3V CMOS outputs as well as I_{off} Supports Partial-Power-Down Mode Operation

■ DEVICE FUNCTIONAL MODES

INPUTS		INPUT/OUTPUT	FUNCTION
$\overline{OE}$	S	A	
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	H_i-Z	Disconnect

Note: H=High Voltage Level, L=Low Voltage Level, H_i-Z: High-Impedance.

■ APPLICATION INFORMATION

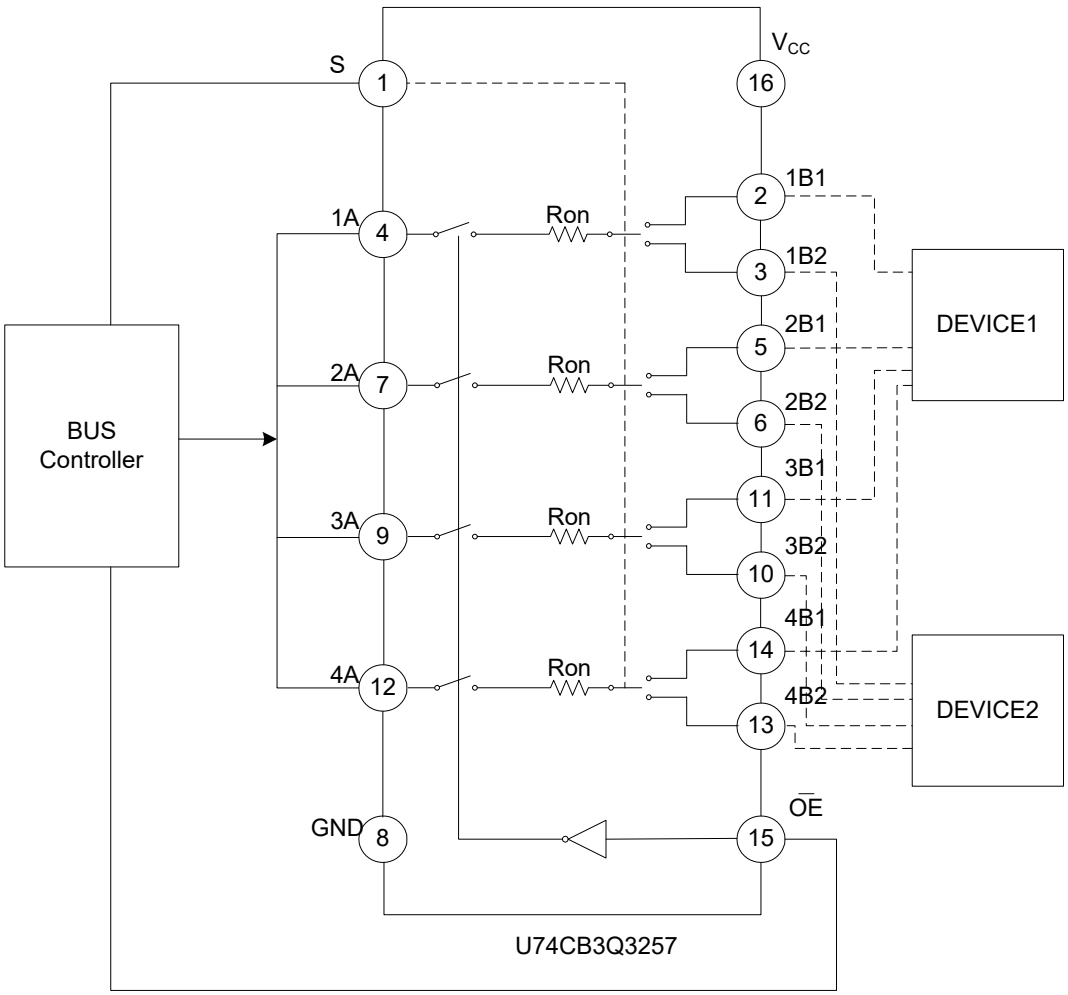
The UTC **U74CB3Q3257** can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. The application shown here is a4-bit bus being multiplexed between two devices. the OE and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires less than 4 bits, be sure to tie the Aside to either high or low on unused channels.

■ POWER SUPPLY RECOMMENDATIONS

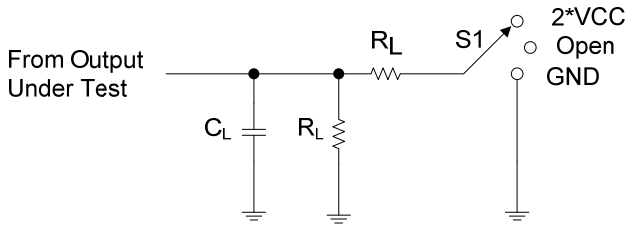
The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the Absolute Maximum Ratings table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1μF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01μF or 0.022μF capacitoris recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1μFand1μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

■ TYPICAL APPLICATION CIRCUIT



■ TEST CIRCUIT AND WAVEFORMS

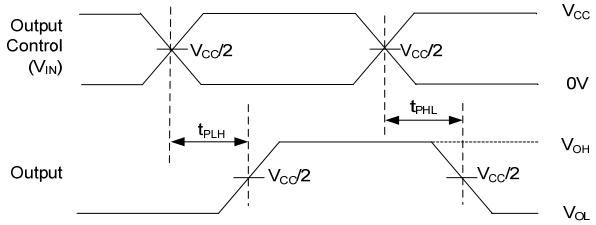


TEST	S1
t_{PLZ}/t_{PZL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

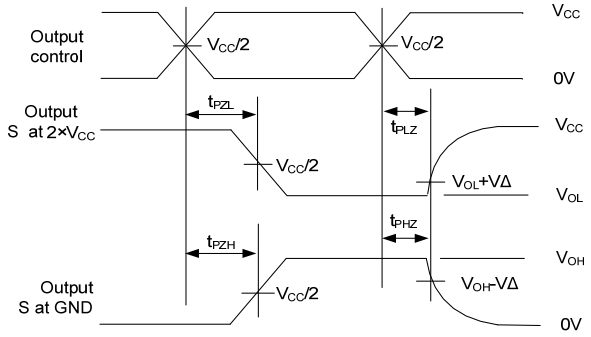
LOAD CIRCUIT

Note: C_L includes probe and jig capacitance.

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
t_{PD}	2.5V±0.2V	Open	500Ω	V_{CC} or GND	30pF	
	3.3V±0.3V	Open	500Ω	V_{CC} or GND	50pF	
t_{PLZ} / t_{PZL}	2.5V±0.2V	2×V_{CC}	500Ω	GND	30pF	0.15V
	3.3V±0.3V	2×V_{CC}	500Ω	GND	50pF	0.3V
t_{PHZ} / t_{PZH}	2.5V±0.2V	GND	500Ω	V_{CC}	30pF	0.15V
	3.3V±0.3V	GND	500Ω	V_{CC}	50pF	0.3V



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O=50Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as tdis.
6. t_{PZL} and t_{PZH} are the same as ten.
7. t_{PLH} and t_{PHL} are the same as t_{PD}(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
8. All parameters and waveforms are not applicable to all devices.