



F9NM65

Preliminary

Power MOSFET

9.0A, 650V N-CHANNEL SUPER-JUNCTION MOSFET

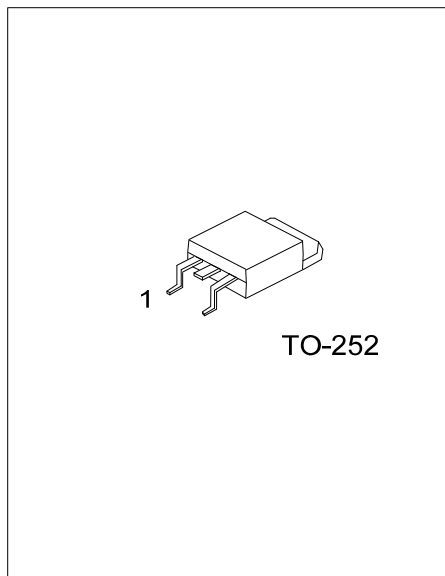
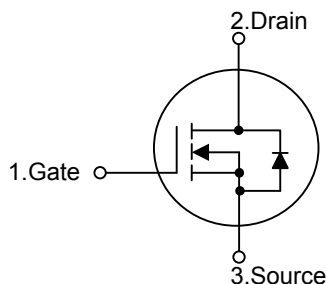
DESCRIPTION

The **UTC F9NM65** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} \leq 0.58 \Omega$ @ $V_{GS}=10V$, $I_D=4.5A$
- * High switching Speed
- * 100% avalanche tested
- * Improved dv/dt capability

SYMBOL



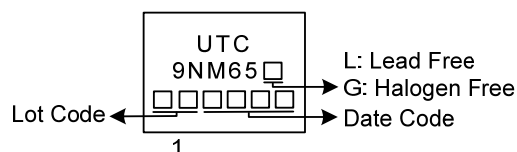
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
F9NM65L-TN3-R	F9NM65G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

F9NM65G-TN3-R		(1)Packing Type	(1) R: Tape Reel
		(2)Package Type	(2) TN3: TO-252
		(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current ($T_C=25^\circ\text{C}$)	Continuous	I_D	9	A
	Pulsed (Note 2)	I_{DM}	36	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	270	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	5.8	V/ns
Power Dissipation		P_D	62	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L=100\text{mH}$, $I_{AS}=3.2\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.

4. $I_{SD} \leq 9.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2 (Note)	$^\circ\text{C}/\text{W}$

Note: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

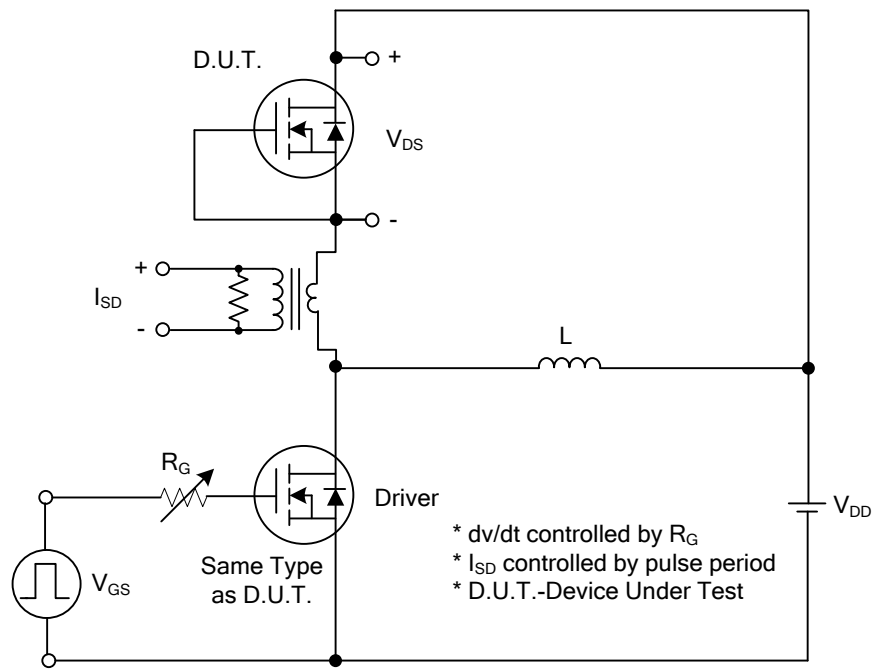
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	650			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =650V, V _{GS} =0V			10	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V			+100	nA
	Reverse		V _{GS} =-30V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =4.5A			0.58	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1.0MHz		570		pF
Output Capacitance		C _{OSS}			100		pF
Reverse Transfer Capacitance		C _{RSS}			6		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 2)		Q _G	V _{DS} =520V, V _{GS} =10V, I _D =9.0A (Note 1, 2)		33		nC
Gate to Source Charge		Q _{GS}			10		nC
Gate to Drain Charge		Q _{GD}			11		nC
Turn-ON Delay Time (Note 2)		t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =9.0A, R _G =25Ω (Note 1, 2)		8		ns
Rise Time		t _R			20		ns
Turn-OFF Delay Time		t _{D(OFF)}			74		ns
Fall-Time		t _F			50		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				9	A
Maximum Pulsed Drain-Source Diode Forward Current (Note 1)		I _{SM}				36	A
Drain-Source Diode Forward Voltage (Note 2)		V _{SD}	I _S =9.0A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _S =9.0A, V _{GS} =0V,		110		ns
Reverse Recovery Charge (Note 1)		Q _{rr}	dl _F /dt = 100 A/μs		430		nC

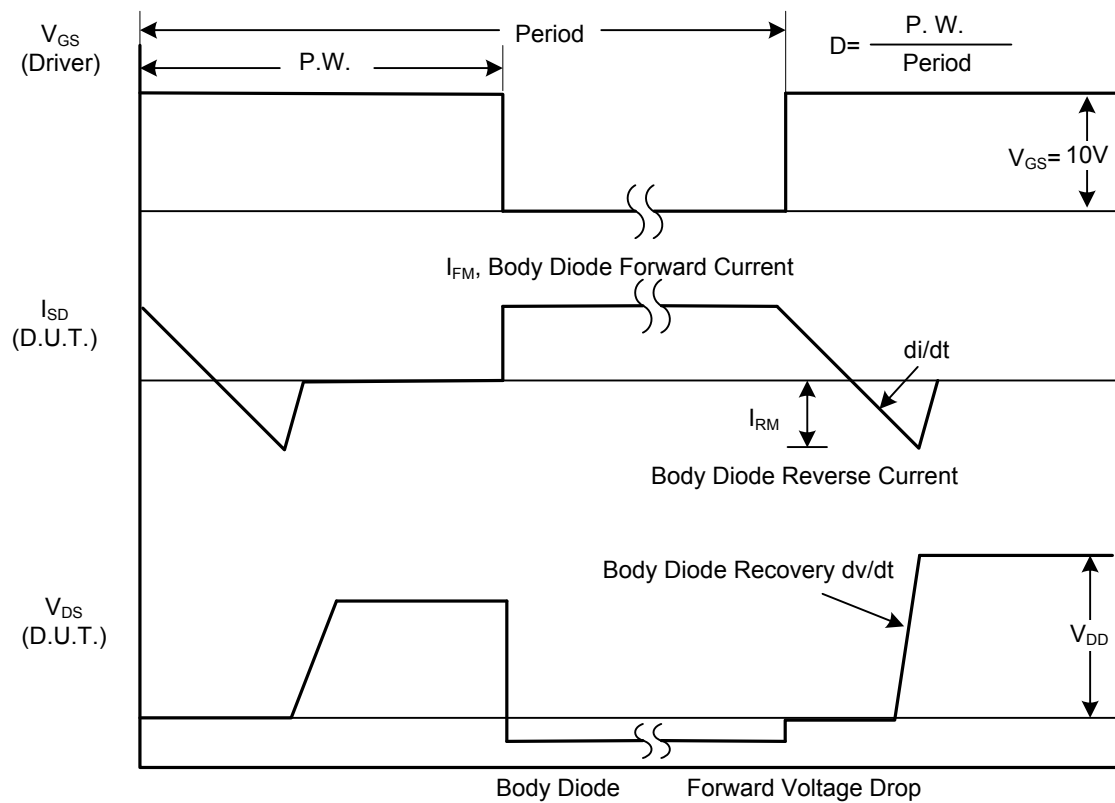
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

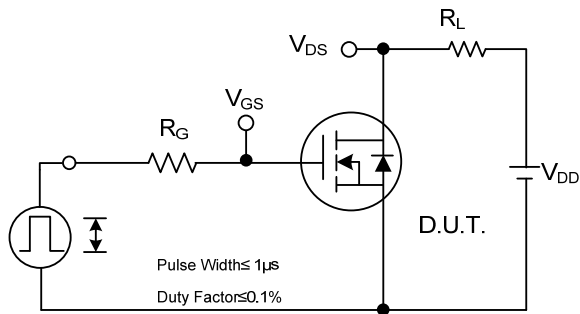


Peak Diode Recovery dv/dt Test Circuit

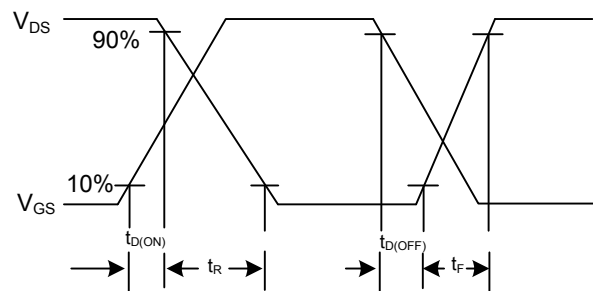


Peak Diode Recovery dv/dt Waveforms

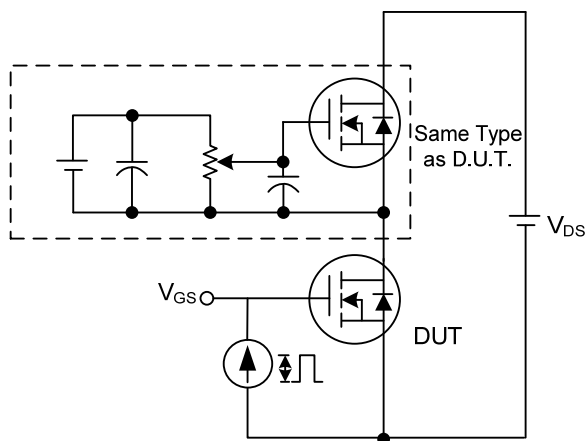
■ TEST CIRCUITS AND WAVEFORMS



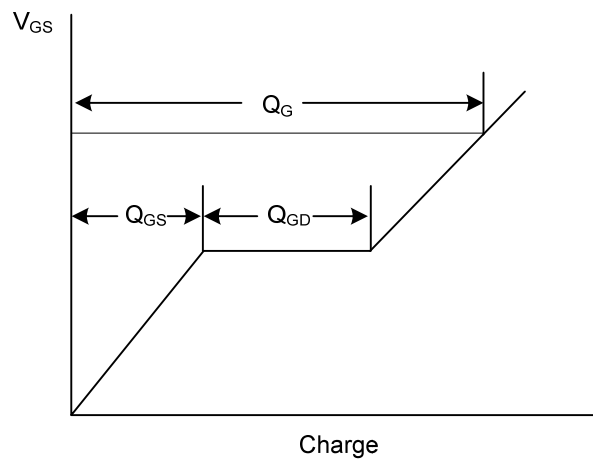
Switching Test Circuit



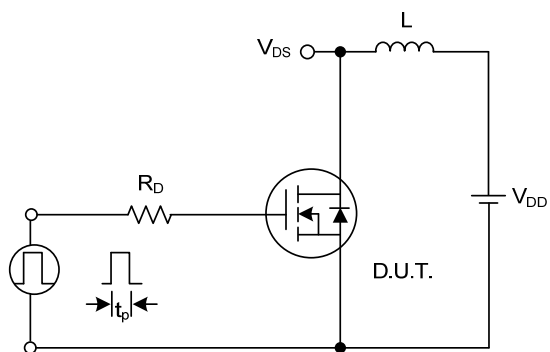
Switching Waveforms



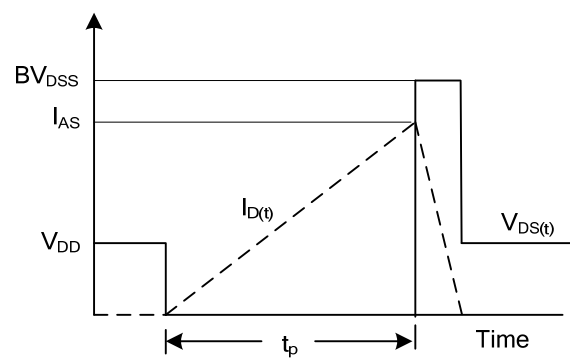
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.