

**50NM65SZ-U3**

Preliminary

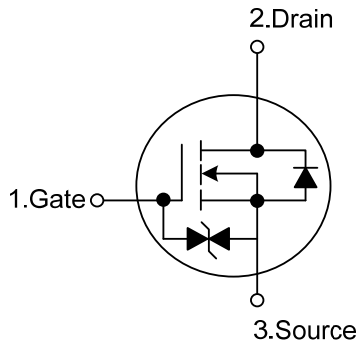
Power MOSFET

**50A, 650V N-CHANNEL
SUPER-JUNCTION MOSFET****DESCRIPTION**

The **UTC 50NM65SZ-U3** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

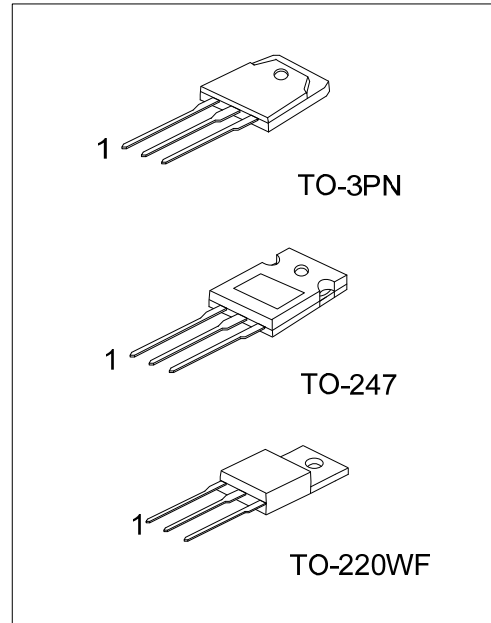
- * $R_{DS(ON)} \leq 70 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=25\text{A}$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness
- * With ESD Protected

SYMBOL**ORDERING INFORMATION**

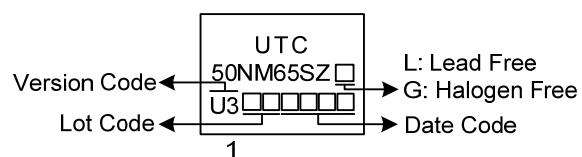
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
50NM65SZL-U3-TW1-T	50NM65SZG-U3-TW1-T	TO-220WF	G	D	S	Tube
50NM65SZL-U3-T3N-T	50NM65SZG-U3-T3N-T	TO-3PN	G	D	S	Tube
50NM65SZL-U3-T47-T	50NM65SZG-U3-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

50NM65SZG-U3-TW1-T	(1)Packing Type (2)Package Type (3)Version Code (4)Green Package	(1) T: Tube (2) TW1: TO-220WF, T3P: TO-3P, T47: TO-247 (3) Version U3 (4) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V _{DSS}	650	V
Gate-Source Voltage			V _{GSS}	±20	V
Drain Current	Continuous	T _C =25°C	I _D	50	A
	Pulsed (Note 2)		I _{DM}	150	A
Avalanche Energy	Single Pulsed (Note 3)		E _{AS}	100	mJ
Peak Diode Recovery dv/dt (Note 4)			dv/dt	2.9	V/ns
Power Dissipation		TO-220WF	P _D	44	W
		TO-247		210	W
		TO-3PN		235	W
Junction Temperature			T _J	+150	°C
Storage Temperature			T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 100\text{mH}$, $I_{AS} = 1.4\text{A}$, $V_{DD} = 90\text{V}$, $R_G = 25\Omega$ Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220WF	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
	TO-247		40	$^{\circ}\text{C}/\text{W}$
	TO-3PN		30	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-220WF	θ_{JC}	2.84	$^{\circ}\text{C}/\text{W}$
	TO-247		0.595	$^{\circ}\text{C}/\text{W}$
	TO-3PN		0.53	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±10	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =25A			70	mΩ
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1MHz		3619		pF
Output Capacitance	C _{OSS}			816		pF
Reverse Transfer Capacitance	C _{RSS}			0.01		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =520V, V _{GS} =10V, I _D =50A (Note 1, 2)		101		nC
Gate-Source Charge	Q _{GS}			21		nC
Gate-Drain Charge	Q _{DD}			37		nC
Turn-On Delay Time (Note 1)	t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =50A, R _G =25Ω (Note 1, 2)		54		ns
Turn-On Rise Time	t _R			35		ns
Turn-Off Delay Time	t _{D(OFF)}			197		ns
Turn-Off Fall Time	t _F			61		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				50	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =50A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t _{rr}	I _S =30A, V _{GS} =0V, dI _F /dt=100A/μs		480		nS
Body Diode Reverse Recovery Charge	Q _{rr}			8739		nC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

D.U.T.

V_{DS}

I_{SD}

L

V_{DD}

Driver

R_G

V_{GS}

Same Type as D.U.T.

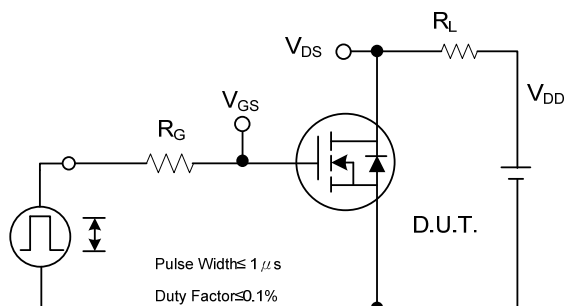
- * dv/dt controlled by R_G
- * I_{SD} controlled by pulse period
- * D.U.T.-Device Under Test

Timing diagram for a MOSFET switching a load inductor. The diagram shows three waveforms: V_{GS} (Driver), I_{SD} (DUT), and V_{DS} (DUT).

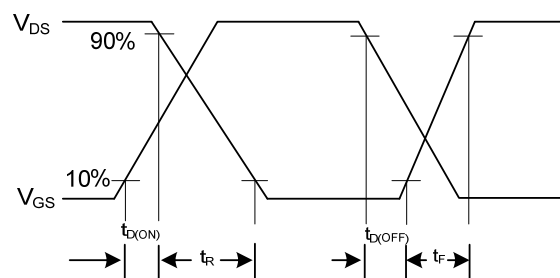
- V_{GS} (Driver): A pulse-width modulated signal. The duty cycle is defined as $D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$. The pulse height is $10V$.
- I_{SD} (DUT): The source-drain current. It shows a forward current I_{FM} (Body Diode Forward Current) during the pulse. During the fall time, it shows a reverse current I_{RM} (Body Diode Reverse Current) with a di/dt label.
- V_{DS} (DUT): The drain-source voltage. It shows a voltage drop V_{SD} (Body Diode Forward Voltage Drop) during the fall time. The recovery voltage is labeled V_{DD} (Body Diode Recovery dv/dt).

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QW-R205-A30.a

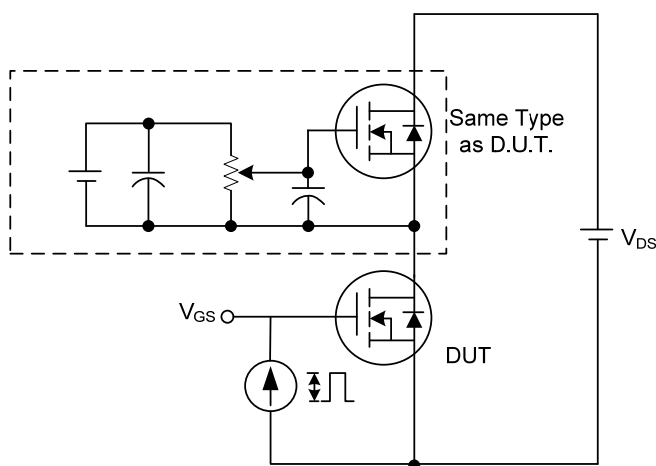
■ TEST CIRCUITS AND WAVEFORMS



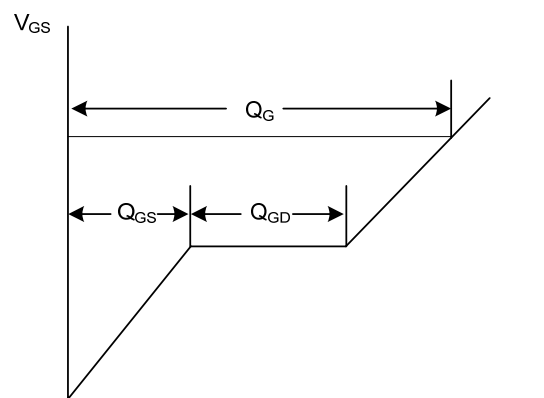
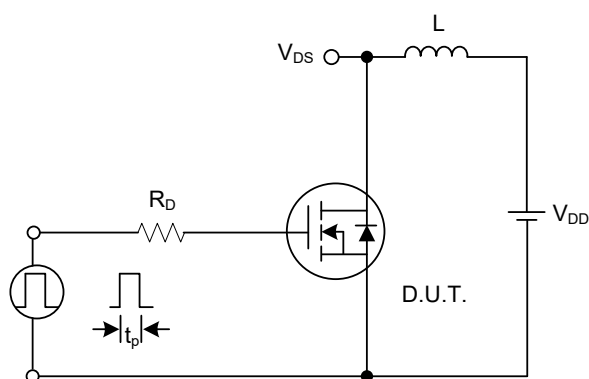
Switching Test Circuit



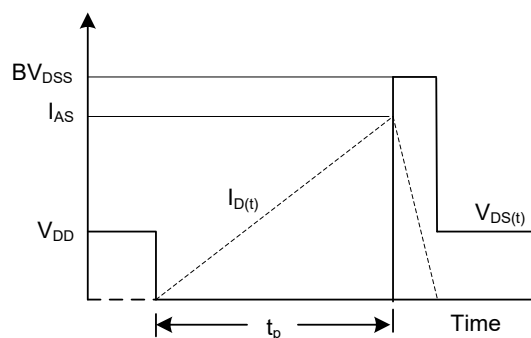
Switching Waveforms



Gate Charge Test Circuit

Charge
Gate Charge Waveform

Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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