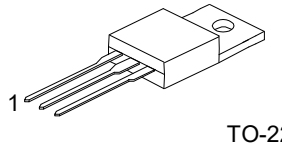
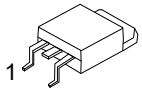
12A, 60V N-CHANNEL POWER MOSFET



TO-220



TO-252

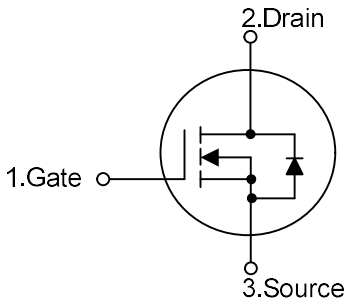
■ DESCRIPTION

The UTC **UT12N06** is an N-channel mode Power MOSFET using UTC's advanced technology to provide customers with minimum on-state resistance with extremely high dense cell design, rugged avalanche characteristics and less critical alignment steps.

■ FEATURES

* $R_{DS(on)} \leq 0.10\ \Omega$ @ V_{GS} = 10V, I_D = 6.0A
  $R_{DS(on)} \leq 0.12\ \Omega$ @ V_{GS} = 5.0V, I_D = 6.0A
* High switching speed
* Low gate charge

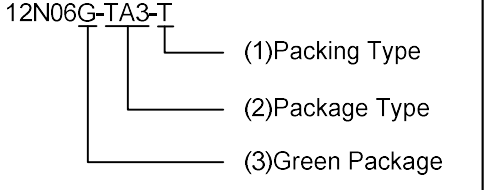
■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N06L-TA3-T	12N06G-TA3-T	TO-220	G	D	S	Tube
12N06L-TN3-R	12N06G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

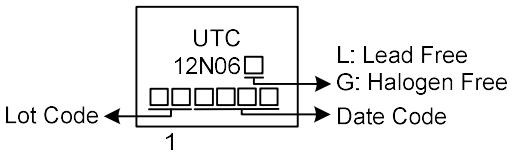


(1) T: Tube, R: Tape Reel

(2) TA3: TO-220, TN3: TO-252

(3) G: Halogen Free and Lead Free L: Lead Free

■ MARKING



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■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

ARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage (V_{GS}=0)			V_{DSS}	60	V
Drain-Gate Voltage (R_{GS}=20KΩ))			V_{DGR}	60	V
Gate-Source Voltage			V_{GSS}	±20	V
Drain Current	Continuous	T_C = 25°C	I_D	12	A
		T_C = 100°C		8.5	A
	Pulsed (Note 2)		I_{DM}	48	A
Power Dissipation		TO-220	P_D	100	W
		TO-252		30	W
Derating Factor		TO-220		0.8	W/°C
		TO-252		0.2	W/°C
Peak Diode Recovery dv/dt (Note 3)			dv/dt	15	V/ns
Avalanche Energy (Note 4)			E_{AS}	100	mJ
Junction Temperature			T_J	+150	°C
Storage Temperature			T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L = 10mH, I_{AS} = 6.0A, V_{DD}=50V, R_G = 25Ω, Starting T_J = 25°C.
4. I_{SD} ≤ 12A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	°C/W
	TO-252		100	°C/W
Junction to Case	TO-220	θ_{JC}	1.25	°C/W
	TO-252		5 (Note)	°C/W

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=25mA, V_{GS}=0V	60			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=6.0A		0.08	0.10	Ω
			V_{GS}=5.0V, I_D=6.0A		0.10	0.12	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		350		pF
Output Capacitance		C_{OSS}			75		pF
Reverse Transfer Capacitance		C_{RSS}			30		pF
SWITCHING PARAMETERS (Note 1, 2)							
Total Gate Charge		Q_G	V_{DD}=48V, V_{GS}=5.0V, I_D=12A		7.5	10	nC
Gate to Source Charge		Q_{GS}			2.5		nC
Gate to Drain Charge		Q_{GD}			3.0		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=30V, V_{GS}=4.5V, I_D=6.0A, R_G=4.7Ω (Note 1, 2)		10		ns
Rise Time		t_R			35		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			20		ns
Fall-Time		t_F			13		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				12	A
Maximum Body-Diode Pulsed Current		I_{SM}				48	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	I_S=12A, V_{GS}=0V			1.5	V
Body Diode Reverse Recovery Time		t_{rr}	I_S=12A, V_{GS}=0V, di/dt=100A/μs		50		ns
Body Diode Reverse Recovery Charge		Q_{rr}			65		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

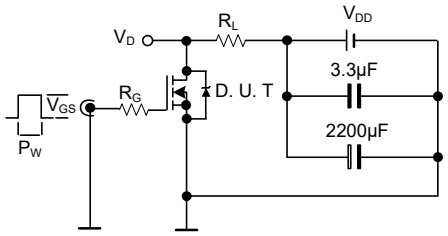


Figure 1. Switching Times Test Circuit for Resistive Load

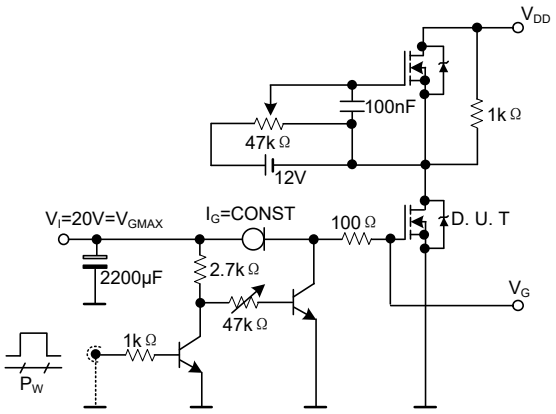


Figure 2. Gate Charge Test Circuit

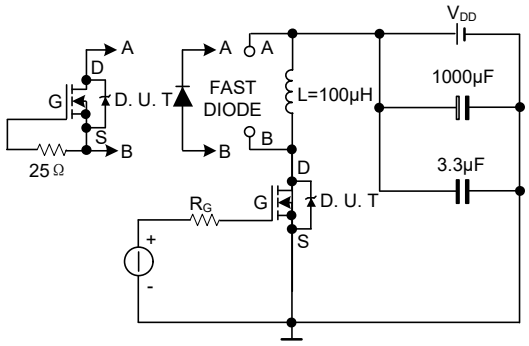


Figure 3. Test Circuit for Inductive Load Switching and Diode Recovery Times

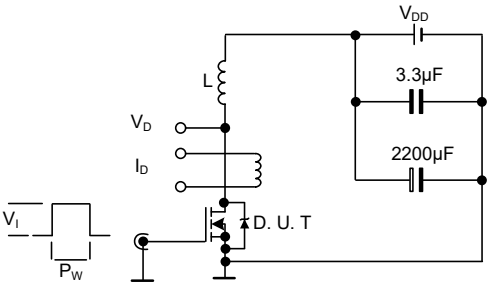


Figure 4. Unclamped Inductive Load Test Circuit

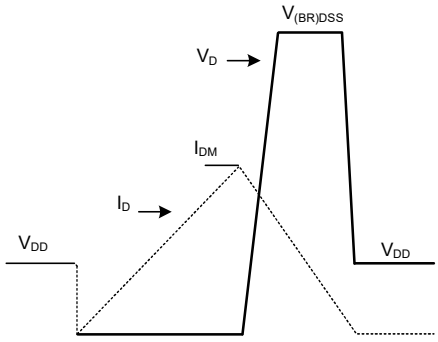


Figure 5. Unclamped Inductive Waveform

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